A 2-Gb/s 0.5-μm CMOS Parallel Optical Transceiver With Fast Power-On Capability

Ping Gui, *Member, IEEE*, Fouad E. Kiamilev, *Member, IEEE*, Xiaoqing Q. Wang, *Student Member, IEEE*, Xingle L. Wang, *Student Member, IEEE*, Michael J. McFadden, *Student Member, IEEE, Student Member, OSA*, Michael W. Haney, *Member, IEEE, Fellow, OSA*, and Charlie Kuznia, *Member, IEEE*

***Abstract*—This paper describes an optical transceiver designed for power-efficient connections within high-speed digital systems, specifically for board- and backplane-level interconnections. A 2-Gb/s, four-channel, dc-coupled differential optical transceiver was fabricated in a 0.5-μm complementary metal–oxide–semiconductor (CMOS) silicon-on-sapphire (SoS) process and incorporates fast individual-channel power-down and power-on functions. A dynamic sleep transistor technique is used to turn off transceiver circuits and optical devices during power-down. Differential signaling (using two optical channels per signal) enables self-thresholding and allows the transceiver to quickly return from power-down to normal operation. A free-space optical link system was built to evaluate transceiver performance. Experimental results show power-down and power-on transition times to be within a few nanoseconds. Crosstalk measurements show that these transitions do not significantly impact signal integrity of adjacent active channels.**

***Index Terms*—Differential links, parallel optical interconnects, power-down, power-on, sleep transistor, transceiver, vertical-cavity surface-emitting laser (VCSEL).**

I. Introduction

POWER-EFFICIENT operation is becoming increasingly important in high-speed digital systems. For example, modern microprocessors from Intel and AMD enable automatic clock throttling while the processor is idle and dynamically power-down unused circuit blocks [1], [2]. For balanced system design, it is important to apply similar power management techniques to interconnections within high-speed digital systems, specifically gigabit parallel-board- and backplane-level interconnections. Without power-efficient interconnects, the power consumption of idle systems will become dominated by interconnects.

Parallel optical links based on vertical-cavity surface-emitting lasers (VCSELs) are an attractive candidate for connections within high-speed digital systems. Compared with their electrical counterparts, they offer inherent advantages in bandwidth–distance product, interconnect density, power consumption, and crosstalk [3]–[5]. However, current parallel optical transceivers do not support efficient power management. Fig. 1 shows a block diagram for one channel of a typical very-short-reach (VSR) parallel optical link [6]. First, parallel input data is encoded to limit the "run length" (consecutive number) of "0" or "1" bits. Then, the data is serialized and transmitted using a single optical channel. The use of limited-run-length data encoding enables the optical receiver to calculate the optimal signal threshold for received optical signals using a simple resistance–capacitance (*RC*) filter circuit. Limited-run-length encoding is also required for proper operation of clock recovery and deserializing functions in the optical receiver. Any deviation from the optimal threshold level (located midway between the maximum and minimum values of the input signal) results in degradation of the channel's bit-error rate (BER).

The use of *RC* filtering to compute the signal threshold requires thousands of bits to be transmitted before the link becomes operational after power-on. This procedure, called *link synchronization*, is normally part of the communication protocol. It is necessary because the *RC* filter requires a long time (relative to the bit period) to compute the correct threshold value. Unfortunately, this means that VSR optical links cannot be powered on quickly, prohibiting efficient power management techniques, such as dynamically powering down unused links, from being applied to parallel optical links.

This paper presents the design details and experimental results for a parallel optical transceiver architecture that supports fast individual-channel power-down and power-on functions. A dynamic sleep transistor technique is used to turn off transceiver circuits and optical devices during power-down. Differential signaling (using two optical channels per signal) enables self-thresholding and allows the transceiver to quickly return from power-down to normal operation. In addition, limited-run-length encoding of optically transmitted signals is not required for proper link operation. A 0.5-μm complementary metal–oxide–semiconductor (CMOS), 2-Gb/s, four-channel, dc-coupled differential optical transceiver has been designed, fabricated, and tested to serve as a vehicle for verifying the proposed architecture. A free-space optical link system was built to evaluate optical link performance. Experimental results show power-down and power-on transition times to be within a few nanoseconds. Crosstalk measurements show that these transitions do not significantly impact the signal integrity of adjacent active channels. To the authors' best knowledge, this

Manuscript received December 30, 2003. This work was supported by the Defense Advanced Research Projects Agency (DARPA) through the Polymorphous Computing Architecture/Reactive Architectures (PCA/RATS) program and through the Center for Optoelectronics at Brown University, Providence, RI, under subcontract 1120-24596.

P. Gui, F. E. Kiamilev, X. Q. Wang, X. L. Wang, M. J. McFadden, and M. W. Haney are with Department of Electrical and Computer Engineering, University of Delaware, Newark, DE, 19716 USA (e-mail: gui@eecis.udel.edu; kiamilev@eecis.udel.edu; wangxiao@eecis.udel.edu; xingle@eecis.udel.edu; mcfadden@eecis.udel.edu; haney@eecis.udel.edu).

C. Kuznia is with Peregrine Semiconductor Corporation, San Diego, CA 92121 USA (e-mail: kuznia@peregrine-semi.com).

Digital Object Identifier 10.1109/JLT.2004.833264

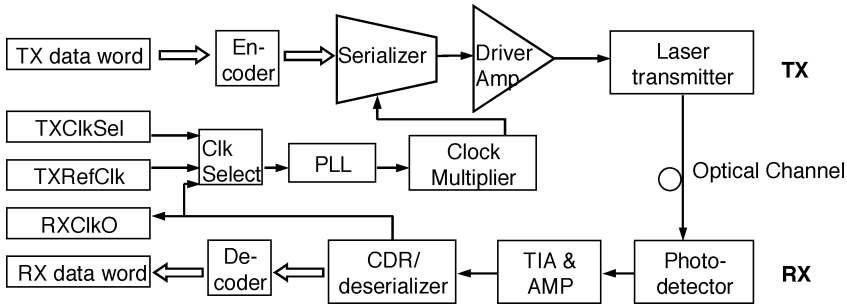


Fig. 1. Block diagram of one channel in a typical VSR optical link.

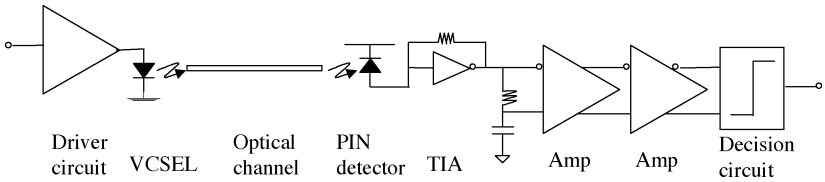


Fig. 2. Block diagram of a single-ended optical link.

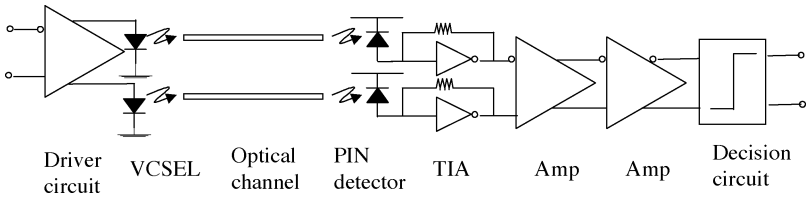


Fig. 3. Block diagram of a differential optical link.

paper describes the fastest power-on and power-down transition for optical links to date.

The remainder of this paper is organized as follows. Section II reviews differential optical signaling. Section III provides the theoretical background for powering down VCSEL devices. Section IV describes the transceiver architecture and circuit design. Section V details the free-space optical link system. Section VI shows the experimental results, and the final section provides conclusions.

II. Differential Versus Single-Ended Optical Links

As shown in Fig. 2, a single-ended optical link consists of one VCSEL device, one optical channel, and one photodetector. At the receiver, an *RC*-filter circuit is usually placed following the transimpedance amplifier (TIA) to generate a threshold voltage based on the input data. Peak BER performance for the link is achieved when the threshold is set to the midpoint between the logic ONE and ZERO levels. However, since the threshold level is subject to the input data pattern, long streams of ONEs or ZEROs cause a drooping effect on the *RC* circuit, which is the threshold voltage drifting from its ideal middle value. To counteract this effect, a large capacitor is used to make the *RC* time constant long (relative to the bit period) so that the variation from the ideal threshold voltage is acceptable for the desired link BER. This results in a long wake-up time (microseconds to milliseconds for gigabit signals) when the link is powered on, and it requires balanced coding of the data to eliminate any long streams of consecutive ONEs or ZEROs.

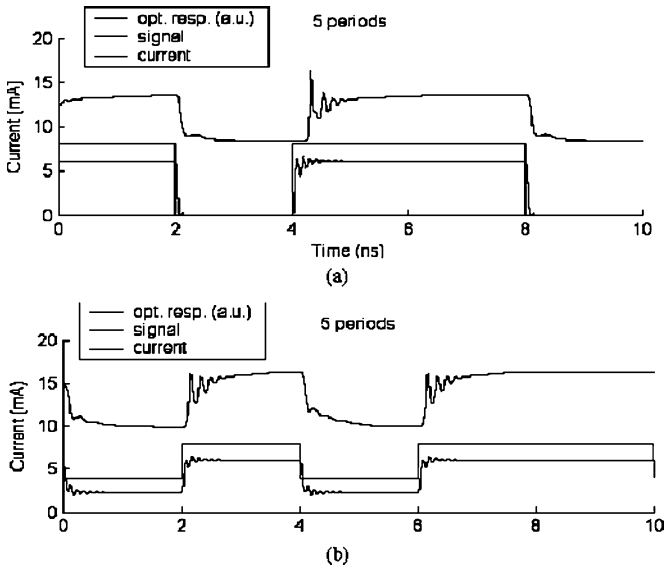


Fig. 4. Simulation of VCSEL turn-on delay. (a) Power-on from zero-bias current. (b) Power-on from above the threshold current.

Fully differential optical links use two optical channels to represent one signal. Fig. 3 shows a block diagram of a transceiver circuit that uses differential optical links. It uses two VCSEL devices at the transmitter, two optical channels, and two photodetectors at the receiver. This concept was first applied to free-space optical interconnect using symmetric self-electrooptic-effect devices (S-SEED) [7]–[11]. There have been reports of all-differential optical receiver for high-bit-rate

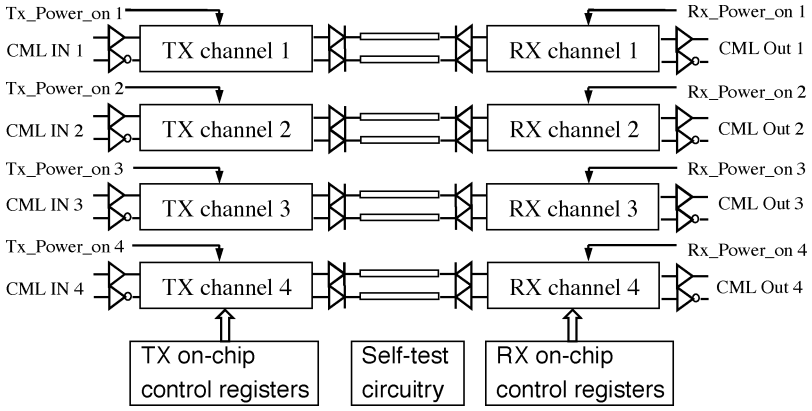


Fig. 5. Block diagram of the IC architecture.

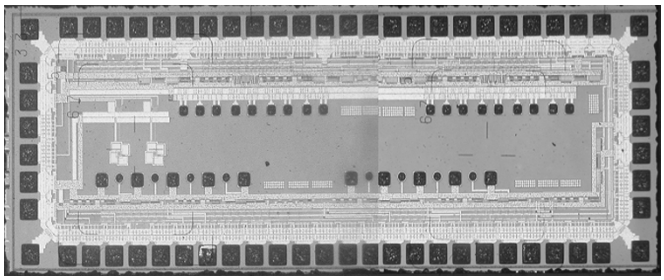


Fig. 6. Microphotograph of the transceiver IC.

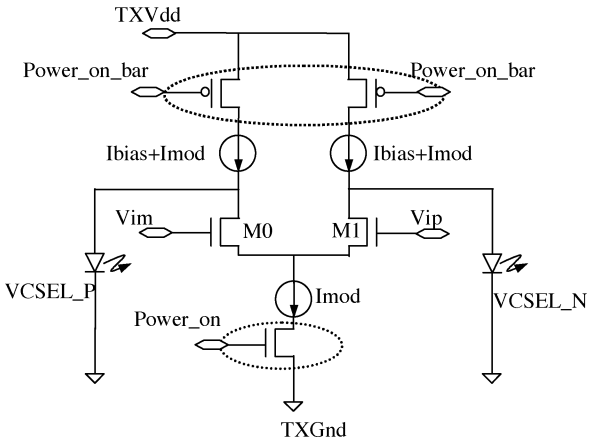


Fig. 7. Schematic of the VCSEL driver circuit with sleep transistor connected in the current path.

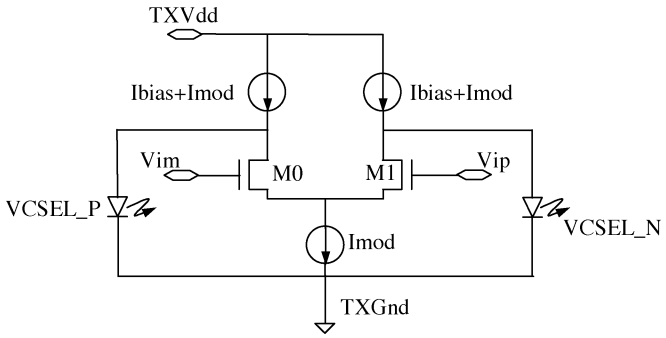


Fig. 8. Schematic of the differential VCSEL driver circuit.

synchronous optical network (SONET) systems [12] and for multiple-quantum-well modulator transceivers [13]. Li and

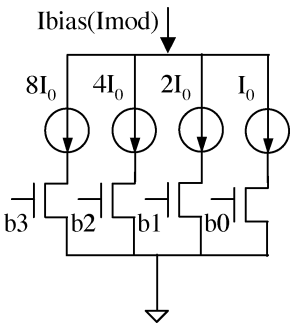


Fig. 9. Binary DAC structure used to set bias and modulation current for individual VCSEL. (b3,b2,b1,b0) are digital control signals.

Stone did a thorough study of differential optical links for high-speed digital systems in [14]–[16]. Although a differential optical link requires twice as many optical devices as a singled-ended link, it has several advantages when used to interconnect high-speed digital systems.

1) Differential links have good noise immunity. Compared with single-ended transceiver circuits, differential links have a higher common-mode noise rejection ratio (CMRR).
2) Differential links generate less power supply noise because they draw constant current from the power supply. Coupled with the previous item, this enables parallel optical transceivers that use differential signaling to scale to a large number of channels [17].
3) Differential links embed the threshold level in the complementary inputs, thus achieving self-thresholding without the need for an *RC*-filter circuit. This simplifies the receiver design.
4) For the same reason as in 3), any type of data (either dc-balanced or with long strings of ONEs or ZEROs) can be transmitted on the differential link without encoding. This reduces the latency and power consumption of the link.
5) Since there is no *RC*-filter circuit needed at the receiver to generate threshold voltage, differential links have almost instant response to incoming data. This enables the link to respond quickly to incoming data after being powered down. This point will be further explored in the next section.

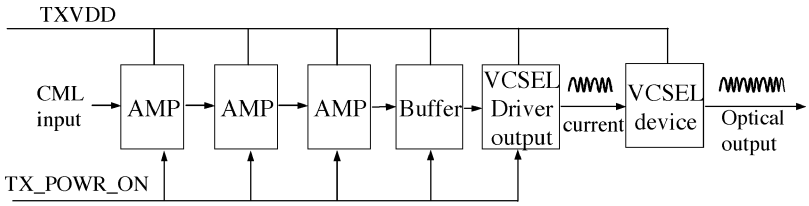


Fig. 10. Block diagram of one transmitter channel with power-on control.

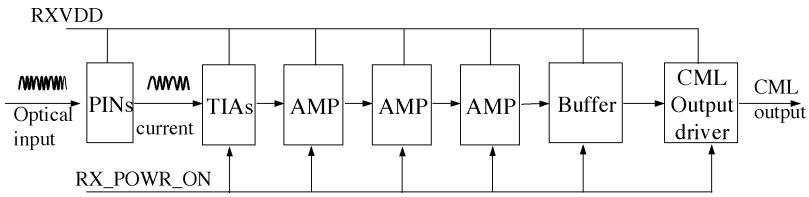


Fig. 11. Block diagram of one-receiver channel receiver with power-on control.

III. VCSEL Device Power-Down

The VCSEL failure rate increases with increasing current density [18]. Thus, powering down the VCSEL device during idle periods not only saves power, but also extends VCSEL lifetime.

There are two ways to power down the VCSEL: 1) turning off the modulation current but keeping the threshold current or 2) completely turning off the current (i.e., zero-bias current). To make a comparison between these two cases, we will now examine a rate-equation-based thermal VCSEL model and simulate the VCSEL turn-on time for both cases [19].

Rate equations describe the time evolution of carrier and photon densities in a laser cavity and are therefore well suited for simulating transient effects. In their simplest form, they consist of a pair of coupled nonlinear differential equations, one for the carrier density and one for the photon density, as shown in ((1a) and (1b)) [5]. In both cases, the rate of increase in density is given by generation rates minus recombination rates. In the photon density case (1b), the generation terms derive from both the spontaneous and the stimulated carrier recombination terms in the carrier density rate equation.

$$\frac{dN}{dt} = \eta_i \frac{I}{qV} - R_{\rm sp} - R_{nr} - g v_g N_p \tag{1a}$$

$$\frac{dN_p}{dt} = \Gamma g v_g N_p + \Gamma \beta_{\rm sp} R_{\rm sp} - \frac{N_p}{\tau_p}. \tag{1b}$$

In these equations, η_i is the injection efficiency, the fraction of terminal current that provides carriers that recombine in the active region; I is the terminal current; q is the electronic charge; $V = \pi a^2 L_a$ is the active region volume; $R_{\rm sp}$ is the spontaneous recombination rate of carriers; $R_{\rm nr}$ is the nonradiative recombination rate; $g v_g N_p$ is the stimulated recombination rate of carriers, in which g is the incremental optical gain in the active material and v_g is the group velocity in the axial direction of the mode in question; Γ is the three-dimensional mode confinement factor; $\beta_{\rm sp}$ is the spontaneous emission factor; and τ_p is the photo lifetime in the cavity. The injection efficiency accounts for current that might be shunted around the active region as well as recombination in the diode depletion region outside of the active region.

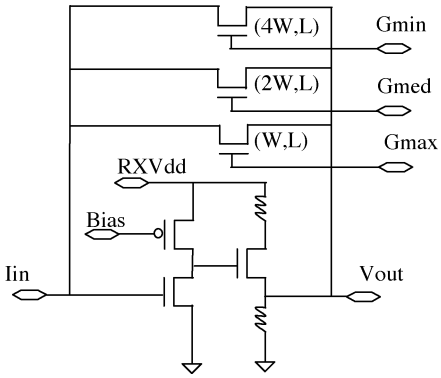


Fig. 12. Schematic of the TIA.

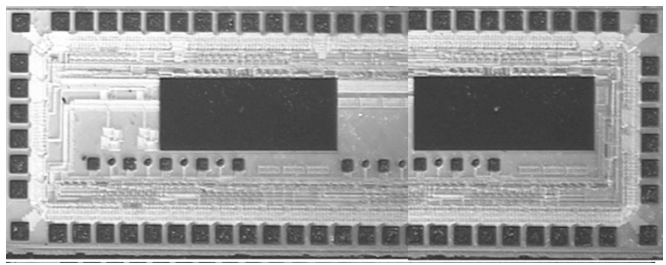


Fig. 13. Microphotograph of the transceiver IC with two 1 × 4 OE devices flip-chip attached at the center of the die.

Fig. 4(a) and (b) shows the simulation results of VCSEL turn-on time (a) from a completely OFF state (zero bias) and (b) from at-threshold current (2.5 mA), respectively.

In both cases, we see the ringing of the optical output. This is due to the dynamic exchange of energy between the electron and photon population in the laser cavity during turn-on [20]. Physically, turning on the laser creates an abrupt rise in the electron population, which then causes a decrease in the photon population as light is emitted. This is countered by another buildup of electrons, which in turn causes another decrease in the photon population, a process that repeats itself iteratively until the number of photons reaches some steady-state value. This phenomenon is most pronounced when the laser is activated very quickly from a completely OFF state to a state above threshold.

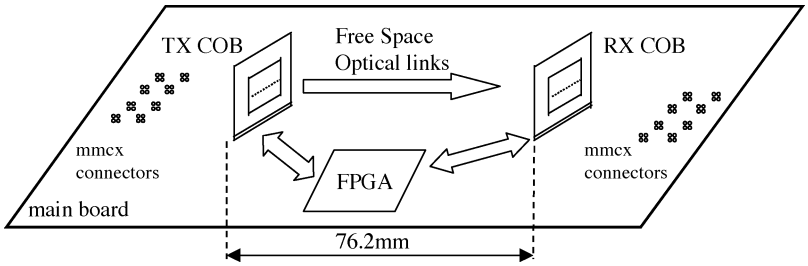


Fig. 14. Schematic of the main board with transmitter and receiver COBs.

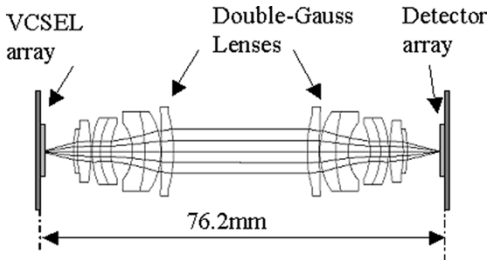


Fig. 15. Schematic of the free-space optical system.

Fig. 16. View of the transceiver IC with OE arrays attached as seen by the camera.

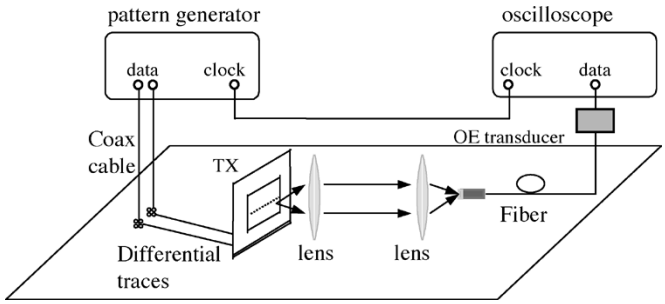


Fig. 17. Experimental setup for transmitter performance evaluation.

As can be seen from the figure, in (b), the turn-on time is almost negligible, in the range of tens of picoseconds, whereas in (a), there is about 250 ps of initial delay before there is any optical output. This delay only happens when the VCSEL is biased below threshold current and can be calculated by

$$T_d = \tau_{\rm sp} \ln \left[\frac{I_p}{(I_p - I_{\rm th})} \right] \tag{1c}$$

where I_p is the peak pulse current [21].

Although the turn-on delay and related jitter are bigger for (a), we implement it as one of the power-down options in our circuit for several reasons.

1) For those VCSEL devices that have a large threshold current, a great amount of power can be saved if the device is powered down with zero bias.
2) From the system point of view, the turn-on delay from zero bias is kept to the minimum by using differential links. In some application, this delay, on the order of nanoseconds, may be small enough to be negligible compared with the latency introduced by the communication protocol at the upper data link level.
3) Since it only occurs once, at the beginning of each string of data, the power savings are worth the small initial turn-on delay.

IV. Transceiver Design

To verify the proposed architecture, a 2-Gb/s, four-channel, dc-coupled differential optical transceiver has been designed and fabricated in a 0.5-μm ultrathin silicon-on-sapphire (UTSi) (SoS) CMOS process.[1] Figs. 5 and 6 show the block diagram and photograph for the transceiver integrated circuit (IC). The chip size is 5 $\times$ 1.5- mm with one transmitter channel occupying 650 $\times$ 75-μm and one receiver channel 740 $\times$ 77-μm.

[1]Peregrine Semiconductor Corp., San Diego, CA, available online at www.peregrine-semi.com

Although differential optical links are being used, the sizes of transmitter and receiver circuits are almost identical to those used in single-ended transceivers.

Since differential circuits are sensitive to device mismatch, care was taken in the layout of the IC. A common-centroid layout technique was used in differential pairs throughout the design to minimize the effect of any threshold mismatches between devices. Dummy polysilicon gates were placed at the edge of active areas to reduce any possible mismatch introduced by the fabrication processing [22]. At the receiver, the dual TIAs were laid out symmetrically and placed as close to each other as possible. There are small digital controllable current sources at the input of each TIA to compensate for any mismatch that might exist. The remainder of this section details the design for key circuit components of the transceiver.

A. Dynamic Sleep Transistor Technique

A dynamic sleep transistor technique is used in microprocessors to turn off unused circuit blocks [23]. We use this technique in our transceiver to implement power-down. A metal–oxide–semiconductor field-effect transistor (MOSFET) switch is inserted in the path of every current source in the circuit to implement power-down/power-up. This MOSFET

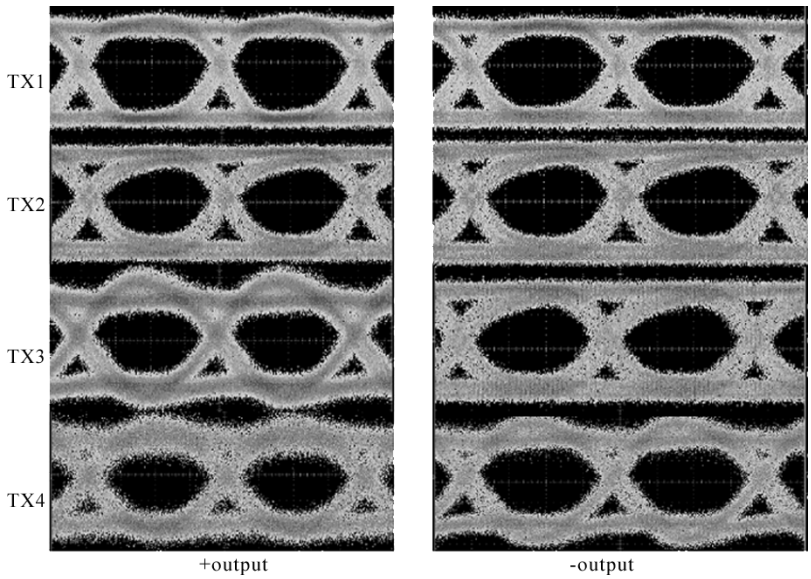


Fig. 18. Eye diagrams for the optical +output and −output of all four VCSEL drivers on one IC at 2.5 Gb/s ($2^{15} - 1$ NRZ pseudorandom pulse pattern).

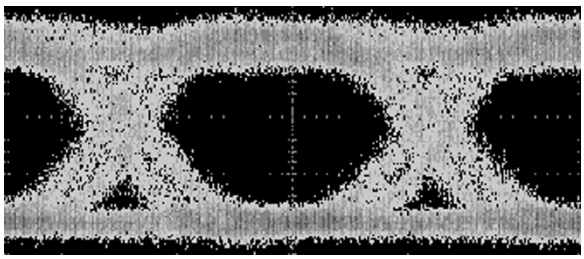


Fig. 19. Eye diagram of one VCSEL output at 3-Gb/s ($2^{15} - 1$ NRZ pseudorandom pulse pattern).

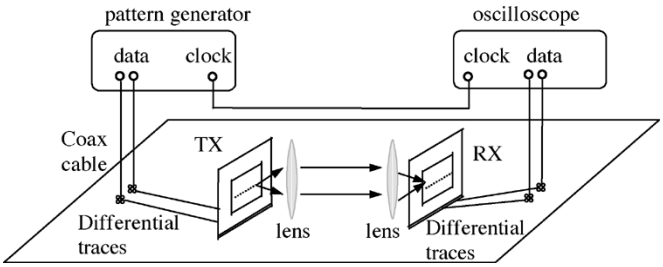


Fig. 20. Experimental setup for link performance measurement.

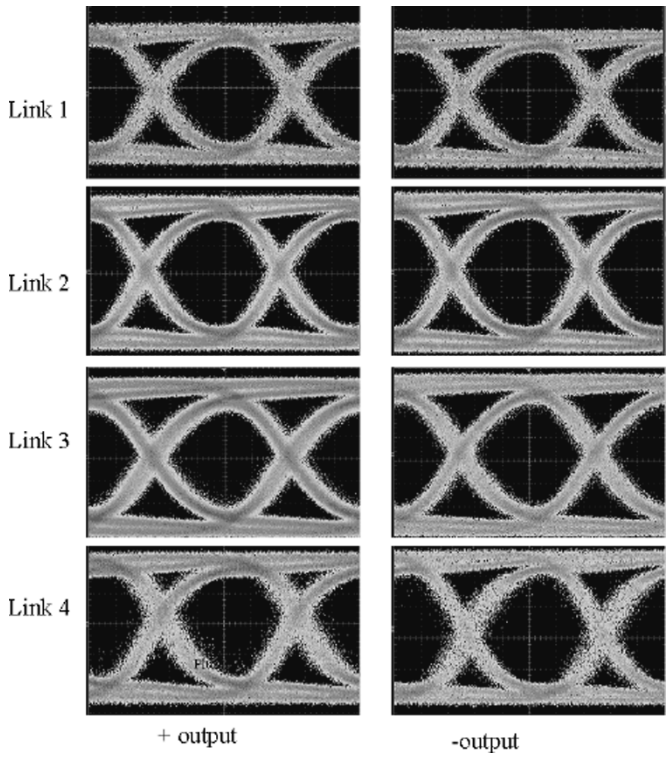


Fig. 21. Eye diagrams for CML electrical outputs for all four channels of one IC running a complete parallel optical link at 2 Gb/s ($2^{15} - 1$ NRZ pseudorandom pulse pattern).

switch is typically large, designed to handle the current that flows through the path with minimum voltage drop. As an example, Fig. 7 shows the schematic of the VCSEL driver circuit with sleep transistors inserted in the current path. The encircled transistors are sleep transistors. When they are turned on, current will flow through the circuit. When they are turned off, the current is cut off, and this part of the circuit is powered down.

Powering down one channel in an array where multiple channels are sharing the same power supply and substrate can produce severe switching noise on the power supply. All the gate output nodes in the circuit that is powered down will be discharged quickly during sleep mode. Significant current spiking is observed at V_{dd} when the circuit is powered on again. For one VCSEL device to switch from the completely OFF state to transmitting signal "1", the current demand from the power supply V_{dd} and the current injection into the ground potential changes from 0 to $(I\mathrm{bias} + I\mathrm{mod})$ over a period of time t_r (rising time of the signal). For a current transient of di/dt, V_{dd} increases by Ldi/dt, while ground potential decreases by Ldi/dt where L is the inductance of bonding wire of the power supply. The total switching noise is linearly proportional to the number of channels as well as the bonding wire inductance and inversely proportional to the rise time of the

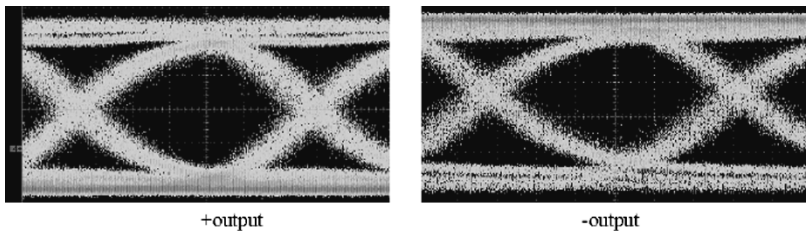


Fig. 22. Complete optical link eye at 2.5 Gb/s ($2^{15} - 1$ NRZ pseudorandom pulse pattern).

signal [15]. This could be a severe problem in conventional single-ended architectures. However, the switching noise is less of a problem for differential links because of their high CMRR. A small amount of decoupling capacitance is effective in eliminating the switching noise [15]. Another factor that works into our advantage is that the sapphire substrate has no parasitic bulk capacitance, thus adding minimum substrate noise into our system.

B. VCSEL Driver Circuit

The VCSEL driver circuit was designed with a current steering structure from a differential amplifier. Fig. 8 shows the schematic of the VCSEL driver circuit where the VCSEL devices are connected to both outputs of the differential amplifier. The modulation current is provided by the current source $I_{\rm MOD}$ and is steered through one of the two arms that is connected to the VCSEL device, forming signal "1" or "0". For example, in the logic "1" state with Vip high and Vim low, $I_{\rm MOD}$ is steered through M1, causing a current of $I{\rm bias}$ to the VCSEL_N and a current of $(I{\rm bias} + I{\rm mod})$ to the VCSEL_P. The current steering nature of the driver allows the total current drawn from the power supply to remain nominally constant at $2(I{\rm bias} + I{\rm mod})$ at all times. Since large optoelectronic (OE) arrays tend to have nonuniform characteristics, it is useful to be able to individually adjust the modulation and bias currents of each channel. This is done using the binary-weighted current digital-to-analog converter (DAC) structure shown in Fig. 9, allowing for individual digital adjustment of each VCSEL modulation and bias current. In our circuit, both the bias current and modulation current can be set in the range of 0–6.75 mA.

The transmitter is designed for a current-mode logic (CML) electrical input. Multiple stages of differential amplifiers are placed before the VCSEL driver to amplify the off-chip CML input signal. Fig. 10 shows the block diagram for one channel of the transmitter. To implement power-down, a digital signal (called *TX_POWER_ON*) is connected to the gates of the sleep transistors present in every stage of the transmitter. There are individual TX_POWER_ON control signals for each transmitter channel in the IC.

C. Receiver Circuit

The receiver consists of two photodetectors, two TIAs, and three stages of differential amplifiers, followed by a buffer stage and a CML output driver (see Fig. 11). The TIA, shown in Fig. 12, is an inverter-based TIA with digital controllable resistance feedback (made with NFETs), allowing different gain settings at the receiver (minimum, medium, or maximum).

Similar to the transmitter, a digital signal (called *RX_POWER_ON*) is connected to the sleep transistors at every stage of the receiver to implement power-down capability. There are individual RX_POWER_ON signals for each receiver channel in the IC.

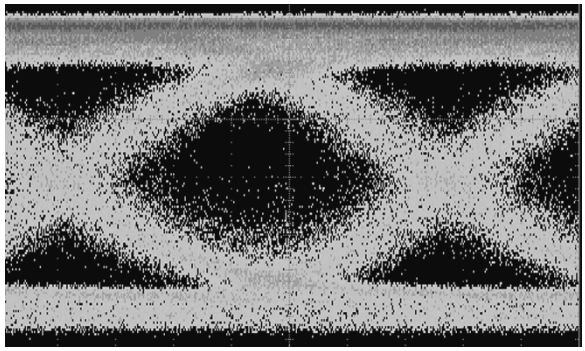


Fig. 23. Complete optical link eye at 3 Gb/s ($2^{15} - 1$ NRZ pseudorandom pulse pattern).

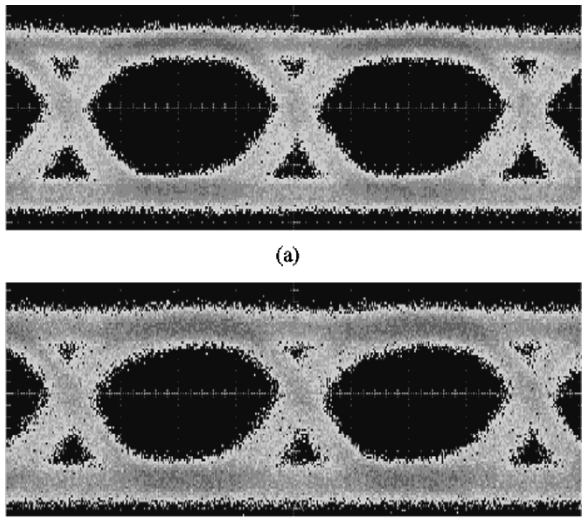
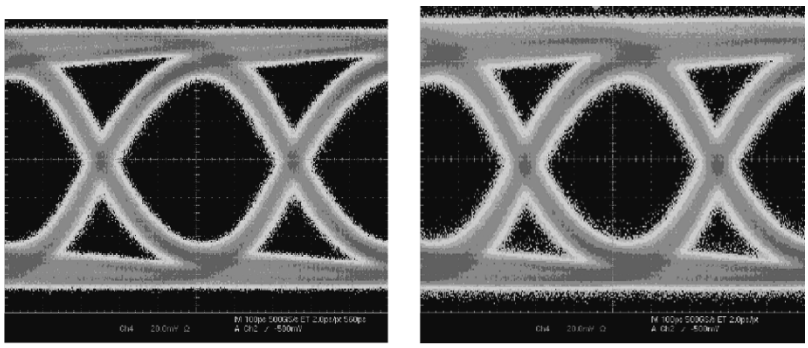


Fig. 24. (a) Eye diagram of VCSEL output at 2.5 Gb/s measured in a normal scenario, with all other transmitter channels being powered on and transmitting data at a gigabit data rate. (b) Eye diagram of VCSEL output at 2.5 Gb/s measured in the worst-case scenario, with all other transmitter channels being simultaneously powered on and off.



(a) (b)

Fig. 25. (a) Eye diagram of receiver output at 2 Gb/s measured in a normal scenario, with all other transmitter and receiver channels being powered on and transmitting data at a gigabit rate. (b) Eye diagram of receiver output at 2 Gb/s measured in the worst-case scenario, with all other transmitter and receivers channels being simultaneously powered on and off ($2^{15} - 1$ NRZ pseudorandom pulse pattern).

V. System Integration

OE devices were attached to the transceiver IC, and a free-space optical link system was constructed to evaluate the transceiver performance. This section describes this system.

A. Optoelectronic Devices

Two 1×4 VCSEL arrays or two 1×4 p-i-n photodetector arrays[2] can alternatively be flip-chip bonded to our transceiver chip, forming four differential optical links. The VCSEL array operates at 850 nm with a threshold current in the range of $0.5 \sim 1$ mA. The differential resistance at $4 \sim 8$ mA is 50 Ω, and the slope efficiency is 0.45 mW/mA. The die size of the VCSEL array is of 1.2×0.45 mm with 250-μm pitch between each channel. The gallium arsenide (GaAs) p-i-n photodiode array operates with a responsivity of 0.5 A/W at 850 nm. The size of the array is 1.055×0.45 mm, and the pitch between devices is also 250 μm.

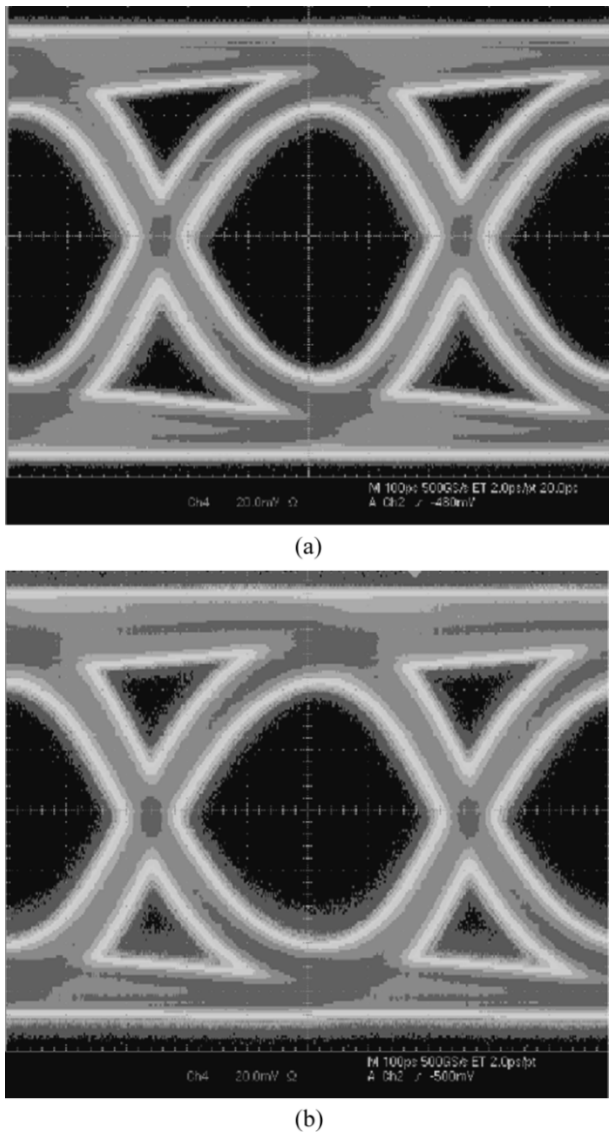
B. Integration Technology

The optical characteristics of the SoS process allow flip-chip integration of VCSELs and photodetectors directly onto the UTSi substrate. The active VCSEL apertures are bonded face-down on the SoS chip with the optical signals passing through the substrate. This allows low parasitic connections to the OE devices in a very simple physical package. Fig. 13 shows the microphotograph of the chip with two 1×4 OE arrays flip-chip bonded to it.

C. Electronic System Design

To test the operation of the IC, we built a printed circuit board (PCB) main board and two chip-on-board (COB) carrier boards, one for the transmitter and one for the receiver. The transceiver ICs with OE arrays attached were wire bonded to the carrier boards. A small rectangular section of the carrier board under the IC was removed to allow optical access to the OE arrays. The carrier boards were then mounted to the main board with high-speed surface-mount connectors. The distance between the carrier boards on the main board is about 76.2 mm. Fig. 14 shows a schematic of the test-bed system.

[2]EMCore Corp., Somerset, NJ, available online at www.emcore.com



(a)

(b)

Fig. 26. (a) Link eye diagram measured at 2 Gb/s after being running for 11 h in a normal scenario, with all the other transceiver channels turned on and transmitting data at a gigabit rate ($2^{15} - 1$ NRZ pseudorandom pulse pattern was used). (b) Link eye diagram measured at 2 Gb/s after being running for 11 h in the worst-case scenario, with all the other transceiver channels repeatedly and simultaneously powered on and off ($2^{15} - 1$ NRZ pseudorandom pulse pattern was used).

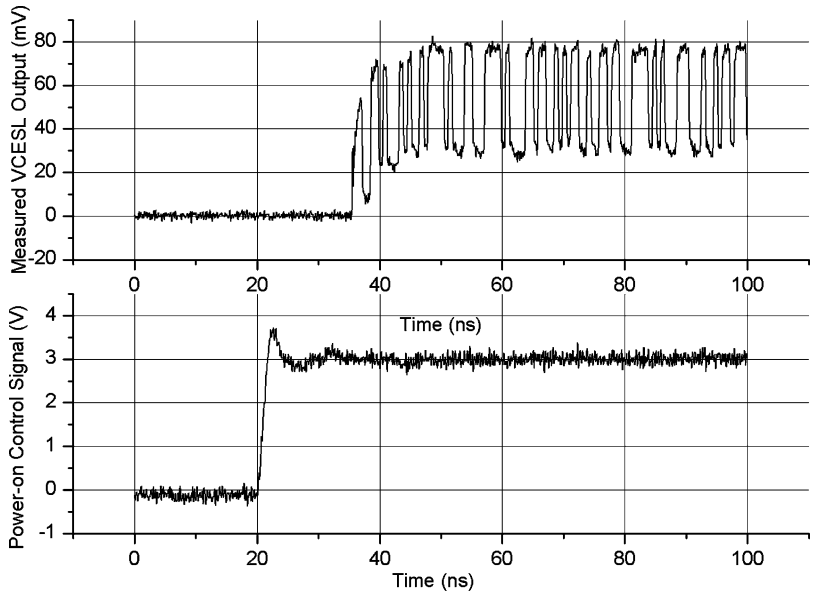


Fig. 27. Transmitter power-on time measurement at 1.5 Gb/s. This is a complete optical link measurement.

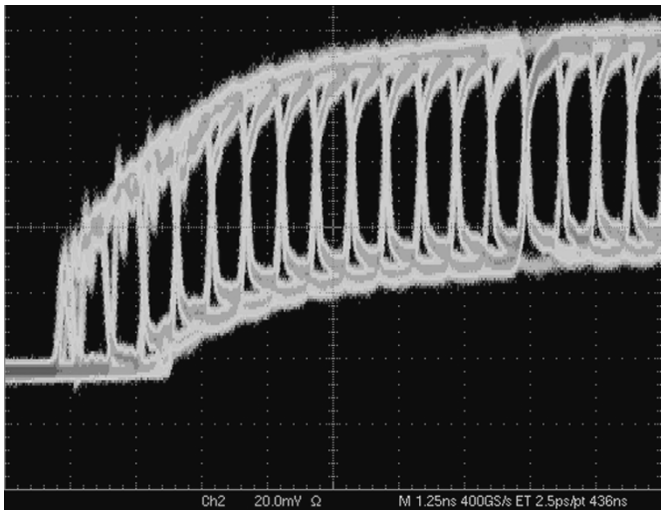


Fig. 28. Transmitter "power-on" eye diagram measurement at 1.5 Gb/s ($2^{21} - 1$ NRZ pseudorandom pulse pattern). This measures the optical output of the transmitter powered on from zero bias.

The main board is an 8× 8-in ten-layer FR4 board. A Xilinx Virtex II Pro FPGA[3] was placed in the center of the main board and was programmed to generate multiple channels of serial data streams at gigabit rate and control logic for the test of the transceiver ICs.

D. Optical System Design

The transmitter and receiver were interconnected using the free-space optical setup shown in Fig. 15. The optical interconnect was performed using two high-resolution seven-element f-2.8 lenses from Universe Kogaku in an infinite conjugate ratio imaging system. Placed at one focal length from the VCSEL array, the first lens collimated the VCSEL beams, while the second lens re-imaged them onto the detector array. Since the optical system was approximately paraxial and the distance between the transmitter and receiver is short, the optical path length (OPL) for each channel is almost identical, and the skew between the different channels is very slight.

The optical system was designed to permit a reflective neutral density filter to be placed between the lenses in order to allow the alignment of the lenses with a camera. Using a color camera that was not sensitive to infrared allowed us to observe the incident beam spots without the problem of charge-coupled device (CCD) blooming because, although the VCSELs peak in the infrared, they have a small percentage of visible spectral content in the red. Fig. 16 shows a view of the transceiver IC with OE detector arrays as seen by the camera. The spots are not in sharp focus in the picture because, due to the small chromatic focal shift of the lenses, the VCSELs had to be shifted slightly out of focus in the visible red in order to be at optimal focus in the infrared.

VI. Experimental Results

A. Transmitter Performance

Fig. 17 shows the experimental setup for transmitter performance measurement. A pseudorandom data sequence [$2^{15} - 1$ nonreturn-to-zero (NRZ) pulse pattern] was generated from the pattern generator and sent to the transmitter. The optical output of the transmitter was captured by a fiber with a commercial 10-G OE transducer connected to the oscilloscope.

Fig. 18 shows the eye diagrams of the optical +output and −output from the VCSEL driver measured for all four transmitted channels of one IC at 2.5 Gb/s. In this measurement, the VCSEL modulation current was set at 3.6 mA, and the bias current at 1 mA, just above the device threshold current. Some transmitter channels were able to operate at 3 Gb/s, as shown in Fig. 19.

[3]Xilinx Corp., San Jose, CA available online at www.xilinx.com

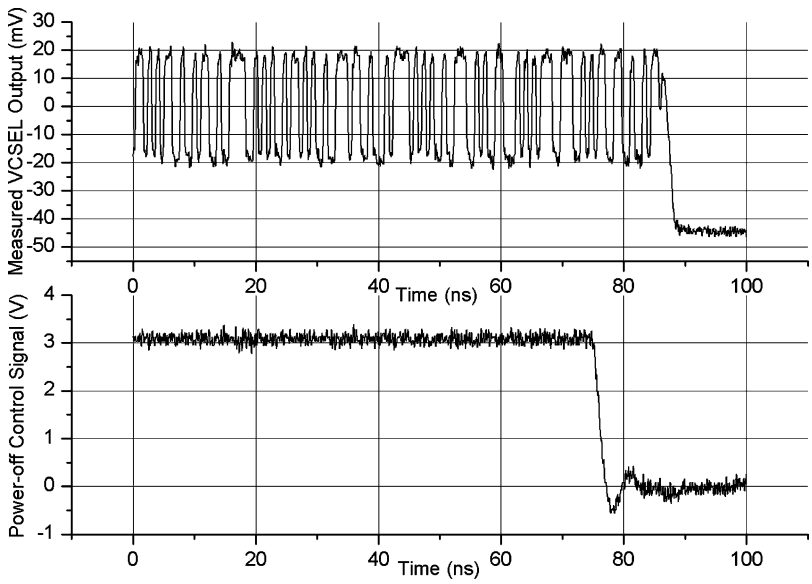


Fig. 29. Transmitter power-down time measurement at 1.5 Gb/s. This is a complete optical link measurement.

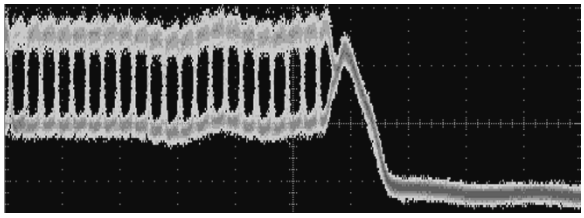


Fig. 30. Transmitter "power-down" eye diagram measurement at 1.5 Gb/s ($2^{15} - 1$ NRZ pseudorandom pulse pattern). This measures the optical output of the transmitter.

B. Link Performance

To test the complete link performance (transmitter, optical link, and receiver), a $2^{15} - 1$ NRZ pulse sequence is generated by a pattern generator and sent to the transmitter. Optical output from the transmitter then goes through the free-space link and is incident on the photodetector in the receiver, which converts the optical signal back to electrical CML format. Fig. 20 shows the experimental setup for the link performance measurement.

Eye diagrams were measured at the receiver CML output. Fig. 21 shows the eye diagrams measured for all four channels of a transceiver IC at data rate of 2 Gb/s.

Some links were capable of running at 2.5 and 3 Gb/s, as shown in Figs. 22 and 23.

C. Crosstalk Measurements

It would be catastrophic if fast power-on and power-down of the individual channels degraded the signal integrity of adjacent active channels. This can occur because cycling power generates on-chip switching noise. Experimental results show that differential links have an excellent common noise rejection ratio, helping active channels operate properly when adjacent channels change power state. Eye diagram and BER measurement were performed for the worst-case scenario where one channel was set up to continuously transmit data while all the other transceiver channels were repeatedly and simultaneously being powered on and off. Fig. 24(a) shows the eye diagram of the VCSEL output of this channel at 2.5 Gb/s with all the other channels in the normal operation states, i.e., transmitting data at 1.5 Gb/s generated by the Virtex II Pro FPGA. As a comparison, Fig. 24(b) shows the eye diagram measured on the same channel, but with all other channels being powered on and off (worst-case scenario). The POWER_ON control signal used for these channels are square waves with a frequency of 500 KHz. This makes the duration of power-on/power-off time to be 1 μs, allowing for transient effects to settle in both the on and off states.

Fig. 25 shows the receiver (link) eye diagrams for this channel (a) with other channels being in the normal operation states and (b) in the worst-case scenario with all the transmitter and receiver being powered on and off.

D. Link Performance for Continuous Operation

The link was operated at 2 Gb/s for 11 h continuously without any errors, achieving a BER of $<$10E-14. The link was also operated under the worst-case scenario at 2 Gb/s for 11 h without any errors. Fig. 26(a) and (b) shows the measured eye diagram after continuous operation for each case.

E. Transmitter Power-On and Power-Down Time Measurement

As mentioned in Section IV, the TX_POWER_ON control signal is connected to every stage of the transmitter. Thus, the system power-on time at the transmitter includes two parts: 1) the power-on time of the circuit stages and 2) the VCSEL device turn-on time.

The transmitter power-on time was measured as the delay between the rising edge of the TX_POWER_ON control signal and the rising edge of first optical pulse at the receiver. The nearest externally measurable point for TX_POWER_ON is at the connector through which the COB is mounted on the main

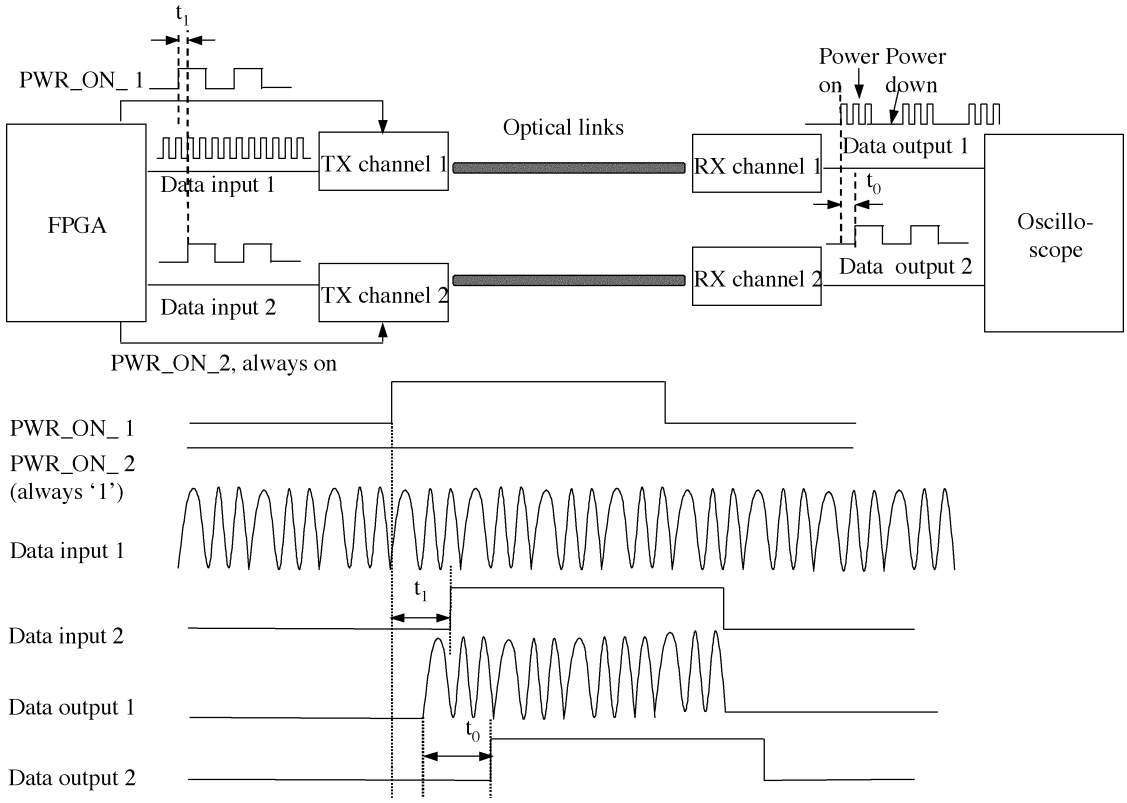


Fig. 31. Transmitter power-on time measurement scheme.

board. Shown in Fig. 17, the VCSEL optical output was captured by a fiber with an OE transducer. Fig. 27 shows the snapshot of these two signals on the scope, and the power-on time is measured to be about 16 ns. Obviously, this delay includes the flight time of the light through the fiber (2-m long), which accounts for approximately 10 ns. It is reasonable, therefore, to conclude that the power-on time is around 6 ns.

The transmitter is powered on and down by the TX_POWER_ON signal, which is a square wave with frequency of 500 KHz. A "power-on" eye diagram of the VCSEL output from zero bias was generated using TX_POWER_ON as the trigger signal (see Fig. 28). From the eye diagram, it is safe to say that the VCSEL output data starts to have good margin within three to four bit periods.

Likewise, the transmitter power-down time was measured as the delay between the falling edge of the TX_POWER_ON control signal and the falling edge of the last optical data output. Fig. 29 shows these two signals captured on the scope. The power-down time is measured to be about 15 ns, including the flight time of the light through the fiber ($\sim$10 ns). Using the same technique in the "power-on" eye diagram measurement, the transmitter "power-down" eye diagram was measured using TX_POWER_ON as the trigger signal. This is shown in Fig. 30. This plot shows that the transmitter stops transmitting in three to four bit periods.

To make a more accurate measurement of the transmitter power-on time from zero bias without having to estimate the propagation delay through the fiber, we constructed a two-channel measurement setup shown in Fig. 31.

The measurement scheme works as follows. normal high-speed data is sent on channel 1, which is powered on and off by a 500-KHz square-wave signal PWR_ON_1. The same PWR_ON_1 signal is sent as the data input to channel 2, which is always powered on. Assuming the two transmitter channels, their optical links, and their receiver channels are identical (e.g., minimal skew), then the data inputs on both channels go through same propagation delays which cancel each other out except for the transmitter power-on time on channel 1 since channel 1 is powered on/off by the PWR_ON_1 signal. Thus, the time delay between the two outputs t_0 gives us the transmitter power-on time. However, the data inputs of channel 2 and the control signal PWR_ON_1 on channel 1, although driven by the same waveform, go though different-length PCB traces on the main board before they arrive at the connector of the COB. Thus, this delay t_1 has to be measured and subtracted from t_0 to give a more accurate measurement of the transmitter power on time.

In our experimental setup, t_1 was measured to be 5.8 ns, and t_0 was measured to be 1.6 ns (repeatable). This gives us a system power-on time of 4.2 ns.

To examine further, the 4.2-ns power-on time includes the VCSEL turn-on delay from zero bias and the VCSEL driver circuit delay from the assertion of TX_POWER_ON signal to the moment when there is at least threshold current coming out of the driver circuit. Simulation results tell us that the circuit delay is about 3.2 ns. Subtracting 3.2 from 4.2 ns, the real VCSEL turn-on delay is about 1 ns (given the resolution

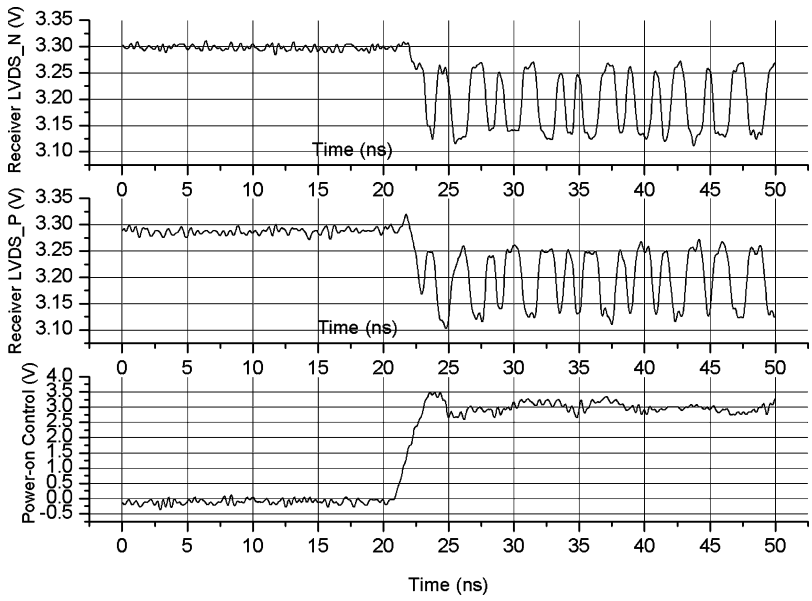


Fig. 32. Receiver power-on time measurement at 1.5 Gb/s. This is a complete optical link measurement. The top two traces show the positive and negative electrical CML output, while the bottom trace shows the RX_POWER_ON control signal.

of the measurement equipment), which is roughly on the same order of those reported for commercial VCSEL devices.

F. Receiver Power-On and Power-Down Time Measurement

The RX_POWER_ON signal is connected in every component of the receiver except the p-i-n photodetector, as shown in Fig. 11. We measured the delay between the rising edge of the RX_POWER_ON signal and the rising edge of the first receiver output as the receiver power-on time. The time was measured to be less than 2 ns, as shown in Fig. 32. Fig. 33 shows the receiver "power-on" eye diagram measured with a periodical RX_POWER_ON as the trigger signal. The plot shows that the receiver becomes fully operational within two to three bit periods after it is powered on.

Likewise, the receiver power-down time was measured as the time from the deassertion of the RX_POWER_ON signal to zero current output at the receiver. Fig. 34 shows the power-down time to be about 1 ns. The receiver "power-down" eye, measured in Fig. 35, shows that the receiver powers down almost instantly, within one bit period.

G. Power Consumption of the Transceiver

Table I below lists the power consumption for one channel of the transmitter and receiver at a data rate of 2 Gb/s. The bias current and modulation current for the VCSEL were set at 1 and 3.6 mA, respectively. The TIA of the receiver was set with minimum gain.

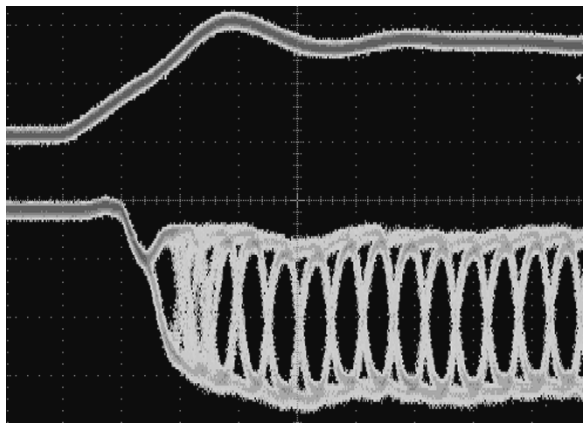


Fig. 33. Receiver "power-on" eye diagram measurement at 1.5 Gb/s ($2^{21}-1$ NRZ pseudorandom pulse pattern). Also shown is the digital power-on signal waveform.

VII. Conclusion

A novel gigabit parallel optical transceiver with fast power-on and power-down capability has been designed, fabricated, and tested. Experimental results have shown that an optical link using this transceiver is able to power-down and/or power-on within a few nanoseconds. This time is many orders of magnitude smaller than that possible with conventional parallel optical transceivers. Differential optical signaling provides self-thresholding capability and makes the fast power-down and power-on capability feasible in parallel optical links, especially where a large number of channels are employed. It is believed that the optical transceiver design introduced in this paper enables a power-efficient operation that is becoming increasingly important in high-speed digital systems.

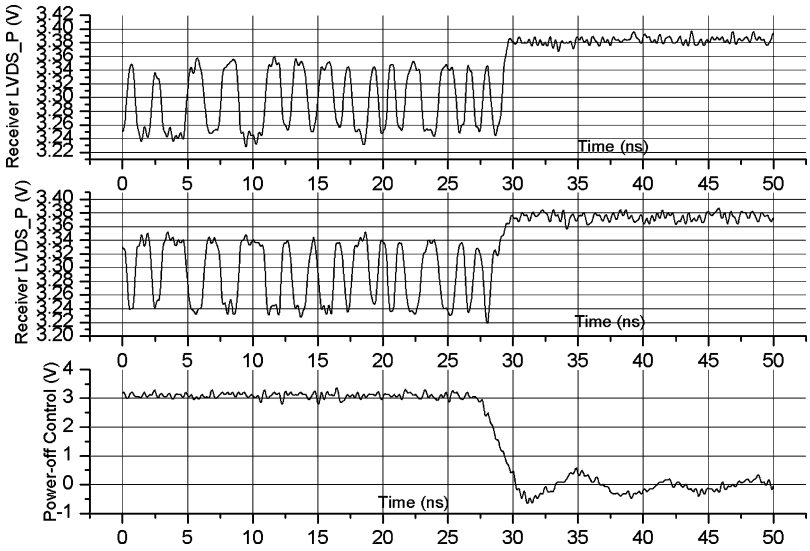


Fig. 34. Receiver power-down time measurement at 1.5 Gb/s. This is a complete optical link measurement. The top two traces show the CML +output and −output, while the bottom trace shows the RX_POWER_ON control signal.

TABLE I
POWER CONSUMPTION OF ONE CHANNEL OF TRANSMITTER AND RECEIVER @ 2 Gb/s

	Transmitter (3.3V)				Receiver (3.3V)				
	CML input	Buffer stage	VCSEL output driver 2*(Ibias+Imod)	Total	TIA	Gain stages (AMPs)	buffer	CML output	Total
Current	3.3mA	2.9mA	9.2mA =(2 *(1+3.6))	15.2mA	1.6mA =2*0.8	3.3mA	2.9mA	7mA	14.8mA
Power	10.9mW	9.6mW	29.8mW	50.3mW	5.28mW	10.9mW	9.6mW	23.1mW	48.8mW

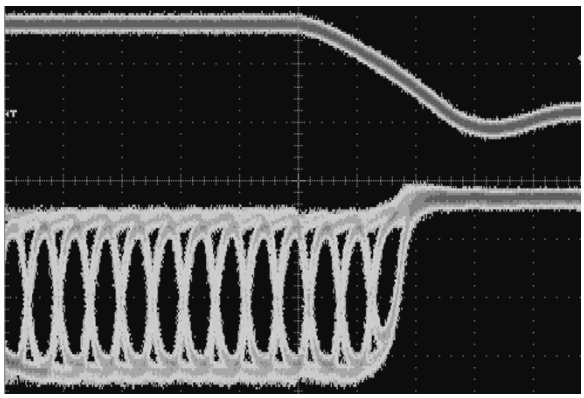


Fig. 35. Receiver "power-down" eye diagram measurement at 1.5-Gb/s ($2^{21} - 1$ NRZ pseudo random pulse pattern). Also shown is the digital RX_POWER_ON signal waveform.

ACKNOWLEDGMENT

The authors would like to thank the Defense Advanced Research Projects Agency (DARPA) and the Center for Optoelectonics at Brown University, Providence, RI, for their support.

REFERENCES

[1] "AMD Athlon 64 FX Processor," Advanced Micro Devices Corp., Publication #30 431, Rev. 3.00, Sept. 2003.

[2] "Intel Pentium M Processor," Intel Corp., Publication #252 612-002, Rev. 2.00, June 2003.

[3] N. Savage, "Linking with light," *IEEE Spectrum*, vol. 39, pp. 32–36, Aug. 2002.

[4] E. Griese, "A high performance hybrid electrical-optical interconnection technology for high-speed electronic systems," *IEEE Trans. Advanced Packag.*, vol. 24, pp. 375–383, Aug. 2001.

[5] C. Wilmsen, H. Temkin, and L. A. Coldren, *Vertical-Cavity Surface-Emitting Lasers: Design, Fabrication, Characterization, and Applications*. Cambridge, U.K.: Cambridge Univ. Press, 1999, pp. 1–65.

[6] D. Cunningham and B. Lane, *Gigabit Ethernet Networking*. New York: Macmillan , 1999, pp. 143–181.

[7] A. Dickinson and M. E. Prise, "An integrated free space optical bus," in *Proc. Int. Conf. Computer Design (ICCD)*, 1989, pp. 62–65.

[8] D. A. B. Miller *et al.*, "Novel hybrid optically bistable switch: the quantum well self-electro-optic effect devices," *Appl. Phys. Lett.*, July 1984.

[9] D. A. B. Miller *et al.*, "The quantum well self-electro-optic effect devices: optoelectronic bistability and oscillation and self-linearized modulation," *IEEE J. Quantum Electron.*, vol. 21, pp. 1462–1476, Sept. 1985.

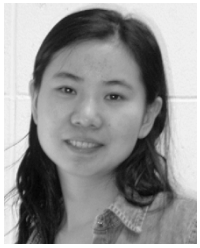
[10] D. A. B. Miller *et al.*, "Integrated quantum well self-electro-optic device: 2×2 array of optically bistable switches," *Appl. Phys. Lett.*, Sept. 1986.

[11] A. L. Lentine *et al.*, "Symmetric self-electro-optic device: optical set-reset latch," *Appl. Phys. Lett.*, Apr. 1988.

[12] G. K. Chang *et al.*, "A direct-current coupled, all differential optical receiver for high-bit-rate SONET systems," *IEEE Photon. Technol. Lett.*, vol. 4, pp. 384–386, Mar. 1992.

[13] T. K. Woodward *et al.*, "1-Gb/s two-beam transimpedance smart-pixel optical receivers made from hybrid GaAs MQW modulators bonded to 0.8-um Silicon CMOS," *IEEE Photon. Technol. Lett.*, vol. 9, pp. 422–424, Mar. 1996.

[14] C. S. Li, H. S. Stone, Y. Kwark, and C. M. Olsen, "Fully differential optical interconnections for high-speed digital systems," *IEEE Trans. VLSI Syst.*, vol. 1, pp. 151–163, June 1993.
[15] C. S. Li and H. S. Stone, "Differential board/backplane optical interconnects for high-speed digital systems—I: Theory," *J. Lightwave Technol.*, vol. 11, July 1993.
[16] C. M. Olsen and C. S. Li, "Differential board-/backplane optical interconnects for high-speed digital systems—II: Simulation results," *J. Lightwave Technol.*, vol. 11, pp. 1250–1262, July 1993.
[17] M. Venditti *et al.*, "Design and test of an optoelectronic-VLSI chip with 540-element receiver-transmitter arrays using differential optical signaling," *IEEE J. Select. Topics Quantum Electron.*, vol. 9, no. 2, pp. 361–379, Mar./Apr. 2003.
[18] B. M. Hawkins *et al.*, "Reliability of various size oxide aperture VCSELs," in *Proc. 52nd IEEE Electronics Components Technology Conf. (ECTC 2002)*, May 2002, pp. 540–550.
[19] M. Jungo. VCSEL Integrated Spatio-Temporal Advanced Simulator. [Online]. Available: http://vistas.sourceforge.net
[20] J. J. Morikuni *et al.*, "The mixed-technology modeling and simulation of optoelectronic microsystems," *J. Modeling Simulation Microsystems*, vol. 1, no. 1, pp. 9–18, 1999.
[21] R. G. Hunsperger, *Integrated Optics: Theory and Technology*, 4th ed. Berlin, Germany: Springer-Verlag, 1995.
[22] A. Hastings, *The Art of Analog Layout*. Englewood Cliffs, NJ: Prentice Hall, 2001.
[23] J. Tschanz *et al.*, "Dynamic-sleep transistor and body bias for active leakage power control of microprocessors," in *Int. Solid-State Circuits Conf. (ISSCC) 2003 Tech. Dig.*.

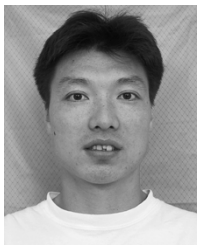


Ping Gui (S'00–M'04) received the B.S. degree in electrical engineering from Northwestern Polytechnic University, Xi'an, China, and the Ph.D. degree in electrical engineering from the University of Delaware, Newark.

In 2004, she joined Southern Methodist University, Dallas, TX, where she is currently an Assistant Professor of electrical engineering. Her research interests include mixed-signal very large scale integration (VLSI) design, optoelectronic integrated circuit (IC) design, and high-speed systems integration.

Dr. Gui is a Member of IEEE Solid-State Circuits Society and the IEEE Lasers & Electro-Optics Society (LEOS).

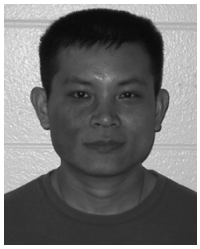
Fouad E. Kiamilev (M'92) was formerly on the faculty of the University of North Carolina at Charlotte (1992–1999). He is currently a Professor with the computer-engineering department at the University of Delaware, Newark. His research group is engaged in the research and development of hybrid and integrated circuits related to optical sensors, communication, and information processing. He has published 26 journal papers, coauthored six patents, and numerous conference papers.



Xiaoqing Q. Wang (S'03) received the B.S. degree in information engineering from Xi'an Electronic Science and Technology University, Xi'an, China, in 1990. He is currently working toward the Ph.D. degree in electrical engineering at University of Delaware, Newark.

From 1994 to 1998, he was with Motorola (China) Electronics, Ltd., where his work focused on developing advanced automatic surface mount and testing technologies. His research interests include very large scale integration (VLSI), mixed-signal design, and high-speed optoelectronics.

Mr. Wang is a Student Member of IEEE Lasers & Electro-Optics Society (LEOS).



Xingle L. Wang (S'00) received the B.S. degree in physics and the M.S. degree in optics, both from Xiamen University, Xiamen, China, in 1992 and 1998, respectively, and the second M.S. degree in electrical engineering from the University of Vermont, Burlington, in 2002. He is currently working toward the Ph.D. degree in electrical and computer engineering with University of Delaware, Newark.

His research interests are mixed-signal design and modeling and high-performance complementary metal–oxide–semiconductor interconnect circuits.

Michael J. McFadden (S'02) received the B.S. degree in electrical engineering from George Mason University. Fairfax, VA, in 2000. He is currently working toward the Ph.D. degree in electrical engineering at the University of Delaware, Newark.

He is currently a Research Assistant in the Photonic Architectures Center, University of Delaware, Newark. His research is currently focused on multiscale optical interconnects for intrachip global communication.

Mr. McFadden is a Student Member of the Optical Society of America (OSA) and the IEEE Lasers & Electro-Optics Society (LEOS). He received an Outstanding Performer Award from the Defense Advanced Research Projects Agency (DARPA) MTO in 2001 for his contributions to the PWASSP ACTIVE-EYES project. He has participated in the IEEE LEOS Workshop on Interconnections within High-Speed Digital Systems for several years and is a General Chair for the 2005 workshop.

Michael W. Haney (M'80) received the B.S. degree in physics from the University of Massachusetts in 1976, the M.S. degree in electrical engineering from the University of Illinois in 1978, and the Ph.D. degree in electrical engineering from the California Institute of Technology, Pasadena, in 1986.

From 1978 to 1986, he was with General Dynamics, where his work ranged from the development of electrooptic sensors to research in photonic signal processing. In 1986, he joined BDM International, Inc., where he became a Senior Principal Staff Member and the Director of Photonics Programs. In 1994, he joined George Mason University, Fairfax, VA, as an Associate Professor of Electrical and Computer Engineering. In 2001, he moved to the University of Delaware, Newark, where he is a Professor of Electrical and Computer Engineering. His research activities focus on the application of photonics to new computing, switching, and signal processing architectures.

Dr. Haney is a Fellow of the Optical Society of America (OSA) and a Member of the IEEE Communications Society and the IEEE Lasers & Electro-Optics Society (LEOS). He has chaired and co-chaired several technical conferences and is a previous Chairman of the IEEE Communications Society's Technical Committee on Interconnections within High-speed Digital Systems.

Charlie Kuznia (S'87–M'87) received the B.S. degree from the University of Minnesota and the M.S. and Ph.D. degrees from the University of Southern California, Los Angeles, all in electrical engineering.

He formerly served as a Professor of Electrical Engineering at the University of Southern California. He has 12 years of research experience in the design and construction of optoelectronic systems and networks. He provides technical oversight to the design of the optomechanical module for interfacing optoelectronic components flip-chip-bumped on UTSi circuitry to fiber-array connectors. He has more than 25 technical publications in the areas of integrated optoelectronic/very large scale integration (VLSI) systems, free-space and fiber-optic interconnects, and diffractive microlens array and grating design.