



TECHNICAL PROGRAM

38th International Symposium on Multiple-Valued Logic

May 22-23, 2008



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3:45-5:15 PM - Session 3B

Computer Arithmetic

Junkins 113

High-level design of multiple-valued arithmetic circuits based on arithmetic description language	Y. Watanabe, N. Homma, K. Degawa, T. Aoki, T. Higuchi
Semirigid Equivalence Relations on a Finite Set	M. Miyakawa, M. Pouzet, I.G. Rosenberg, H. Tatsumi

6:30-8:30 PM

Meadows Museum Reception and Tour

SMU Meadows Museum

8:30 PM

Hotel Shuttle Busses depart from SMU Meadows Museum**Friday, May 23, 2008**

8:00-8:30AM

Registration Desk Opens

Junkins Foyer

8:30-9:30 AM

Keynote Address

Junkins 101

Foundations of Higher Radix Numeric Computation,
Dr. David W. Matula, Professor, Southern Methodist University

9:30-10:00 AM

Coffee/Tea Break

Huitt-Zollars Pavillion

10:00-12:00 PM - Session 4A

Quantum Computing I

Junkins 101

Minimization of Quaternary Galois Field Sum of Products Expression for Multi-Output Quaternary Logic Function using Quaternary Galois Field Decision Diagram	M.H.A. Khan, N.K. Siddika, M.A. Perkowski
A Qualitative Modal Representation of Quantum Register Transformations	A. Masini, L. Vigano, M. Zorzi
On the Data Structure Metrics of Quantum Multiple-valued Decision Diagrams	D.Y. Feinstein, M.A. Thornton, D.M. Miller
Superposed Quantum State Initialization Using Disjoint Prime Implicants (SQUID)	D. Rosenbaum, M.A. Perkowski

10:00-12:00 PM - Session 4B

Fuzzy Logic and Soft Computing

Junkins 113

Generalized Modus Ponens Based on Linguistic Modifiers in a Symbolic Multi-valued Framework	S.Bel Hadj Kacem, A. Borgi, K. Ghedira
Soft Computing Methods for Prediction of Replication Origins in Caudoviruses	R. Cruz-Cano, I. Aizenberg
Default reasoning with imperfect information in multivalued logics	D. Stamate
Classification of Fastest Quaternary Linearly Independent Arithmetic Transforms	B. Falkowski, C. Fu

12:00-1:15 PM

Lunch

Umphrey Lee Ballroom

1:30-3:00 PM - Paper Session 5A

Circuits II

Junkins 101

A 3/7-Level Mixed-Mode Algorithmic Analog-to-Digital Converter	K. Akutagawa, K. Machida, T. Waho
Fine-Grain Multiple-Valued Reconfigurable VLSI Using Universal-Literal-Based Cells	N. Okada, M. Kameyama
Multiple-Valued Logic Using 3-state Quantum Dot Gate FETs	J. Chandy, F.C. Jain

Paper Session 5B

Nanoscale and Quantum Computing

Junkins 113

Projective Measurement-based Logic Synthesis of Quantum Circuits	M. Lukac, M.A. Perkowski
Multiple-Valued Logic Memory System Design Using Nanoscale Electrochemical Cells	T. Manikas, D. Teeters
Quantum Logic Implementation of Unary Arithmetic Operations	M. A. Thornton, D.W. Matula, L. Spenner, D.M. Miller

3:00-3:30 PM

Coffee/Tea Break

Huitt-Zollars Pavillion

3:30-5:00 PM - Session 6A

Reversible Logic

Junkins 101

Reversible Realization of Quaternary Decoder, Multiplexer, and Demultiplexer Circuits	M.H.A. Khan
Exact Synthesis of Elementary Quantum Gate Circuits for Reversible Functions with Don't Cares	D. Große, R. Wille, G.W. Dueck, R. Drechsler
RevLib: An Online Resource for Reversible Functions and Reversible Circuits	R. Wille, D. Große, L. Teuber, G.W. Dueck, R. Drechsler

3:30-5:00 PM - Session 6B

Spectral Techniques II

Junkins 113

Properties and Computational Algorithm for Fastest Quaternary Linearly Independent Transforms	C.C. Lozano, B.J. Falkowski, T. Luba
Hybrid Reed-Muller-Haar Transform and its Application in Reduction the Spectral Representations of Logic Functions	S. Minasyan, J. Astola, K. Egiazarian, R.S. Stankovic´
Remarks on Bandwidth and Regularities in Functions on Finite non-Abelian Groups	R.S. Stankovic´, J. Astola

5:00-6:00 PM

Plenary Session

Junkins 101

6:30-10:00 PM

Symposium Banquet

Southfork Ranch

Shuttle busses depart from Junkins to Southfork Ranch and return to hotels after banquet ends.**Saturday, May 24, 2008****17th International Workshop on Post-Binary ULSI Systems**

9:00-9:05 AM

Welcoming Remarks

Junkins 101

9:05-10:05 AM

Paper Session I

Junkins 101

High-speed data transmission techniques using raised cosine approximation signaling	Y. Yuminaka, Y. Tsubota
High-level Synthesis of Asynchronous Circuits and Its Optimization	A. Matsumoto, T. Yoneda, T. Hanyu
On the Potential of CMOS Recharged Semi-Floating Gate Devices used in Balanced Ternary Logic	H. Gundersen

10:05-10:20 AM

Coffee/Tea Break

Huitt-Zollars Pavillion

10:20-11:40 PM

Paper Session II

Junkins 101

An Ultrahigh-Speed Full Adder Using Resonant-Tunneling Logic Gates	T. Waho, H. Okuyama, T. Ebata, R. Kato
Power Analysis of RSA Processors with High-radix Montgomery Multipliers	N. Homma, A. Miyamoto, T. Aoki, A. Satoh
The affine gates and affine polarities for quantum arrays with small costs	S. Hossain, M. Perkowski
Using Fuzzy Quantum Logic to learn facial gestures of a Schrodinger Cat puppet for robot theatre	A. Raghuvanshi, M. Perkowski

12:00-1:15 PM

Lunch

Umphrey Lee Ballroom