Design and Optimization of Multi-GHz CMOS LC Voltage-Controlled Oscillators

Chih-Ming Hung

Mixed Signal Wireless Communication Semiconductor Group
Texas Instruments, MS 8728, Dallas, TX 75243
• Motivation

• Passive Components
  + High-Q Capacitors
  + High-Q Varactors
  + On-Chip Spiral Inductors

• Voltage-Controlled Oscillators (VCOs)
  + 1-GHz VCOs
  + 5.5-GHz VCOs
  + How high of frequency can we reach using a CMOS process?

• Conclusions
Motivation

Effects of LO phase noise in a transmitter and a receiver

Diagram showing the effects of LO phase noise in a transmitter and a receiver, with components labeled as Antenna, PA, Transmitter, Receiver, Synthesizer, Reference Oscillator, Digital Signal Processor, IF MoDem, and Data/Speaker Microphone. The diagram illustrates the path of signals from the transmitter and receiver, highlighting the impact of nearby transmitters and interferers on the wanted signal.
Motivation

A general block diagram and a typical output spectrum of an integer-N phase-locked loop (PLL) frequency synthesizer
Motivation

Difficulties of attaining low phase noise in an integrated CMOS LC VCO

- High 1/f noise
- Limited Q for passive components
- Low supply voltage -- limited signal swing and tuning range
- Low current consumption

\[ L(\Delta \omega) = 10 \cdot \log \left\{ \frac{2FkT}{P_s} \cdot \left[ 1 + \left( \frac{\omega_0}{2Q \cdot \Delta \omega} \right)^2 \right] \cdot \left( 1 + \frac{\omega_0}{|\Delta \omega|} \right) \right\} \]
Motivation

What do we need to build a low-phase-noise VCO?
Passive Components

• Requirements
  + High Q
  + Low cost -- no extra process steps, area-efficient
  + Good linearity
  + Easy to implement

Problem: lossy silicon substrate

• MOS Capacitors \( Q \propto \frac{1}{\omega} \)

• \( P^+ \)-Nwell Varactors \( Q \propto \frac{1}{\omega} \)

• Layout Optimization for Transistors

• On-Chip Spiral Inductors
MOS Capacitor

\[ R_s = \frac{1}{3} \times \frac{1}{2} \times \frac{1}{2} \times \frac{1}{N} \times \left( R_{nw, p} \times \frac{L}{W} + R_{poly, p} \times \frac{W}{L} \right) \]

\[ Q = \frac{1}{\omega CR_s} = \frac{12}{\omega \times c_{unit} \times (R_{nw, p} \times L^2 + R_{poly, p} \times W^2)} \]
MOS Capacitor

0.25-\(\mu\)m CMOS process

- When scaling down the process technology
  - Contact, via and routing metal resistances (especially for large capacitors)
  - Decreased \(C_{\text{acc}}/C_{\text{dep}}\)
  - Leakage current through the gate oxide (for large capacitors)
**P⁺-Nwell Varactor**

0.25-μm CMOS process

![Diagram of P⁺-Nwell Varactor](image)

- **n-well ties (n⁺ diffusion)**
- **p⁺ diffusion**

![Graph of Quality Factor vs. Frequency](image)

**Quality Factor at 0-V junction bias**

\[
R_{var} = \left( R_{nw, p} \times \frac{2 \cdot L}{L + 2 \cdot W} \times \frac{1}{4} + \frac{R_{nw, p}}{28.6} \right) \times \frac{1}{N}
\]

\[
Q_{var} = \frac{1}{\omega R_{var} C_{var}} = \frac{1}{\omega C_{var}} \cdot \frac{N}{R_{nw, p}} \cdot \frac{15.3 \cdot L + 2 \cdot W}{28.6 \cdot (L + 2 \cdot W)}
\]
Varactor Options

- Quality factor requirement
- Gate length vs. minimum active area spacing
- N-well resistance under channel region vs. under FOX region
- Linearity of VCO gain ($k_{vco}$)
Layout Optimization for Transistors

- Improves $Q$ of $C_{gs}$, $C_{gd}$, $C_{gb}$ and $C_{db}$
- Sufficient area of substrate diffusions
- Sufficient number of contacts for substrate diffusions
Layout Optimization for Transistors

Symmetric for cross-couple connection

gate connection of \( M_1 \)

drain connection of \( M_1 \)

gate connection of \( M_2 \)

drain connection of \( M_2 \)

polysilicon

n-well ties

\( p^+ \) diffusion
Inductor

- Patterned-ground shield
  + Decreases $R_{\text{sub}}$
  + Increases overall $Q$
  + Increases $C_p$
  + But not able to reduce the substrate effect

- Limit the area to reduce the substrate effect
- Optimized using half-bandwidth $Q$ method
- Avoid any closed loop surrounding the inductor

Patterned-ground shield:
- Decreases $R_{\text{sub}}$
- Increases overall $Q$
- Increases $C_p$
- But not able to reduce the substrate effect

Limit the area to reduce the substrate effect

Optimized using half-bandwidth $Q$ method

Avoid any closed loop surrounding the inductor
Inductor

- Metals: M3 + M4 + M5 layers
- PGS: polysilicon layer
- Metal width: 6 \( \mu \text{m} \)
- Metal spacing: 1.8 \( \mu \text{m} \) (proximity effect)
- Inductor area: 90 x 90 \( \mu \text{m}^2 \)

\[ L \text{ : 0.95 nH} \]
\[ R_s \text{ : 3.62 \( \Omega \)} \]
\[ C_p \text{ : 47.5 fF} \]
\[ R_{\text{sub}} \text{ : 5.0 \( \Omega \)} \]

Unloaded Q: 7 @ 5.5 GHz
Summary

• **MOS Capacitor**
  + Q of >140 at 5.5 GHz has been achieved using an MOS capacitor structure
  + Inexpensive (naturally available) and area-efficient
  + Easy to implement
  + Controllability of Q
  + High linearity when properly biased
  + Suitable for most applications such as bypassing, (de)coupling and frequency tuning in VCOs

• **Varactor Q of > 60 at 5 GHz and 0-V bias has been achieved**

• **Q of transistor parasitic capacitances are > 25 at 5 GHz which can be further improved**

• **Reasonable inductor Q**
Outline

• Motivation

• Passive Components
  + High-Q Capacitors
  + High-Q Varactors
  + On-Chip Spiral Inductors

• Voltage-Controlled Oscillators (VCOs)
  + 1-GHz VCOs
  + 5.5-GHz VCOs
  + How high of frequency can we reach using a CMOS process?

• Conclusions
Design and Measurement Results of VCOs

• 1-GHz LC VCOs (0.8-\(\mu\)m digital CMOS process)
  + On-chip spiral inductor
  + On-chip spiral inductor + package parasitics

• 5.5-GHz LC VCOs (0.25-\(\mu\)m digital CMOS process)
  + MOS varactor
  + P\(^+\)-nwell diode varactor

• A 25.9-GHz LC VCO implemented in a partial-scaled 0.1-\(\mu\)m bulk CMOS process
1-GHz VCOs

\[ S_{vg} = \frac{K_f}{W \times L \times Cox \times f^A_f} \]

Features:
- Only PMOS transistors are used for lower 1/f and thermal noise
- Phase noise contribution from the bias circuit can be reduced
- Capacitor \( C_{acg} \) is used for reducing the ripple at the source of M3 and phase noise
- Inductively loaded buffers for larger output voltage swing
1-GHz VCOs

VCO using on-chip spiral inductors and package parasitics

Total bond wire inductance:

\[ L_{b,\text{tot}} = \frac{L_{b1} \cdot L_{b2}}{L_{b1} + L_{b2}} + \frac{L_{b3} \cdot L_{b4}}{L_{b3} + L_{b4}} + L_M \]

\[ L_M = L_m, (b1, b2) + L_m, (b3, b4) - L_m, (b1, b3) - L_m, (b1, b4) - L_m, (b2, b3) - L_m, (b2, b4) \]

Total lead inductance:

\[ L_{d,\text{tot}} = L_{d1} + L_{d2} - L_m, (d1, d2) \]

Total inductance = \( L_{b,\text{tot}} + L_{d,\text{tot}} + L_{\text{short}} + L_{\text{spiral}} \)

High Q
Low variability
Die size: 1.2 x 0.8 mm²
Ground-shielded pads
Ground plan
**1-GHz VCOs**

Measurement results -- frequency spectrum and phase noise

Center Frequency: 1.0873 GHz

- $i_{VCO}=4.7$ mA, $V_{control}=V_{DD}=2.7$ V
- Resolution Band Width: 1 kHz
- Video Band Width: 100 Hz

Symbol |  
|  
| $V_{DD}$ (V) | 2.7 | 1.5  
| $i_{VCO}$ (mA) | 4.7 | 4.55 

-126 dBc/Hz @ 600 kHz ($V_{DD}=2.7$ V)  
-125 dBc/Hz @ 600 kHz ($V_{DD}=1.5$ V)
1-GHz VCOs

Measurement results -- frequency tuning range

![Graph showing frequency tuning range](image)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>o</th>
<th>x</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ (V)</td>
<td>2.7</td>
<td>1.5</td>
</tr>
<tr>
<td>$I_{VCO}$ (mA)</td>
<td>4.7</td>
<td>4.55</td>
</tr>
</tbody>
</table>
1-GHz VCOs

Summary

• 0.8-µm CMOS process with 3 metal layers and 0.05 Ω·cm p⁺ substrate
• Performance highlights

<table>
<thead>
<tr>
<th>Packaged VCO</th>
<th>Power Consumption</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Tuning Range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>12.7 mW (2.7, 4.7mA)</td>
<td>-92 @ 10 kHz</td>
<td>-126 @ 600-kHz</td>
</tr>
<tr>
<td></td>
<td>6.8 mW (1.5V, 4.55mA)</td>
<td>-90 @ 10 kHz</td>
<td>-125 @ 600-kHz</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Monolithic VCO</th>
<th>Power Consumption</th>
<th>Phase Noise (dBc/Hz)</th>
<th>Tuning Range (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>66 mW (3 V, 22 mA)</td>
<td>-125 @ 600-kHz</td>
<td>-135 @ 3-MHz</td>
</tr>
</tbody>
</table>

• The first few VCOs exceeding GSM phase noise requirements
• The observed variability of the total inductance for the packaged VCO is low (1%)
• The low close-in phase noise was obtained by utilizing buried channel PMOS devices with low 1/f and thermal noise
5.5-GHz VCOs

A VCO circuit schematic with its bias circuit

Features:

- Only PMOS transistors are used for lower 1/f and thermal noise
- The dependence of $I_{\text{tail}}$ on $V_{\text{DD}}$ is greatly reduced by the bias circuit
- Phase noise contribution from the bias circuit is immeasurable
- Capacitor $C_{\text{acg}}$ is used for reducing the ripple at the source of $M_3$ and phase noise
- Inductively loaded buffers for larger output voltage swing
5.5-GHz VCOs

Measurement results -- phase noise

\[ V_{DD} = 1.5 \, \text{V}, \, I_{\text{tail}} = 4.7 \, \text{mA} \]

-93 dBc/Hz @ 100 kHz
-117 dBc/Hz @ 1 MHz

RBW=10 kHz
VBW=100 Hz
5.5-GHz VCOs

Measurement results -- frequency tuning range

<table>
<thead>
<tr>
<th>Varactor</th>
<th>Phase Noise Flatness</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS</td>
<td>1 dB</td>
</tr>
<tr>
<td>Diode</td>
<td>3 dB</td>
</tr>
</tbody>
</table>

![Graph showing the frequency tuning range of 5.5-GHz VCOs with control voltage.]
5.5-GHz VCOs

- Die size (including pad frame): 581 x 470 \( \mu \text{m}^2 \)
- Empty areas are filled in with p-substrate contacts to reduce substrate coupling while not forming closed loops around the inductors
- Ground-shielded pads are used to reduce substrate coupling
5.5-GHz VCOs

Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25 μm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Type</td>
<td>p⁻ substrate (~8 Ω-cm)</td>
</tr>
<tr>
<td>SSB Phase Noise</td>
<td>-93 @ 100 kHz</td>
</tr>
<tr>
<td>when f₀=5.35 GHz</td>
<td>-117 @ 1 MHz</td>
</tr>
<tr>
<td>(dBc/Hz @ offset)</td>
<td></td>
</tr>
<tr>
<td>Tuning Range</td>
<td>336 MHz (diode)</td>
</tr>
<tr>
<td>(GHz/V_CTL)</td>
<td>310 MHz (MOS)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>7 mW (4.7 mA @ 1.5 V)</td>
</tr>
<tr>
<td>Inductor Q</td>
<td>7 @ 5.5 GHz</td>
</tr>
<tr>
<td>Varactor Q</td>
<td>57 @ 5.5 GHz</td>
</tr>
</tbody>
</table>

- The reported phase noise is >7 dB lower than those of the other published 5-GHz CMOS VCOs
- With 15-mW (6 mA, 2.5 V) power consumption, the phase noise and tuning range can be improved by 2 dB and 70 MHz, respectively
25.9-GHz VCO

• Frequency Limitation
  + Active component: transistor \( f_t \) and \( f_{max} \)
  + Passive components
    - Capacitor \( Q \propto 1/\omega \)
    - Inductor \( Q \propto \omega \)

• Process Technology -- **Bulk** CMOS process
  + 0.35-\( \mu \)m design rules
  + 0.1-\( \mu \)m polysilicon gate length (\( L_{poly} \))
  + p-type substrate with 1-\( \Omega \)-cm substrate resistivity
  + gate oxide thickness: \( \sim 3 \) nm
  + threshold voltage: \( \sim 0.3 \) V for NMOS transistors
  + only 2 metal layers
25.9-GHz VCO

Features:
- Only NMOS transistors are used for higher $f_t$ ($f_{\text{max}}$)
- Noise contribution from the bias circuit can be reduced
- Varactors and bypass capacitors are implemented using a MOS capacitor structure and all bottom plates are ac grounded
- Capacitor $C_3$ is used for reducing the ripple at the source of $M_3$ and phase noise
- Source-follower buffers for driving 50-$\Omega$ load

A VCO circuit schematic
25.9-GHz VCO

- Q > 20 @ 26 GHz
- Sheet resistance
- polysilicon: ~8 $\Omega/\square$
- n-well: ~500 $\Omega/\square$
25.9-GHz VCO

- Non-monotonic C-V characteristic
- $C_{\text{max}}/C_{\text{min}} \sim 1.23$
Polysilicon depletion effect

With polysilicon depletion effect

Ideal C-V curve

Capacitance

Gate Bias

n+ poly gate

gate oxide

n-well

Contact

Contact

p substrate

FOX

FOX

n+ poly gate

silicide

L
25.9-GHz VCO

- Polysilicon depletion effect
- Larger overlap and fringing capacitances ($C_{\text{overlap}} + C_{\text{fringe}} \sim C_{\text{gate}}$ at 0.4-V gate bias) due to small gate area
- Doubling the gate length will increase the $C_{\text{max}}/C_{\text{min}}$ ratio by ~22% but decrease Q by ~17%

![Diagram of a 25.9-GHz VCO](image-url)
25.9-GHz VCO

- Metal layers: M1 + M2
- Metal width: 8 \( \mu \text{m} \)
- Metal spacing: 1 \( \mu \text{m} \)
- Inductor area: 2000 \( \mu \text{m}^2 \)
- Inductance: \( \sim 0.2 \text{ nH} \)
- Q \( \sim 3 @ 26 \text{ GHz} \)
  - Not optimized
  - Only 2 metal layers
  - Large substrate effect due to low substrate resistivity (~1 \( \Omega \)-cm)
25.9-GHz VCO

Measurement results -- frequency spectrum and phase noise

Center Frequency: 25.9GHz

\[ \text{Power (dBm)} \]

\[ \text{Frequency Offset (MHz)} \]

\[ \text{Phase Noise (dBc/Hz)} \]

\[ \text{Frequency Offset (Hz)} \]

\[ \text{Frequency Offset (Hz)} \]

\[ V_{DD} = 1.5 \text{ V}, I_{VCO} = 16 \text{ mA}, I_{\text{buffer}} = 3 \text{ mA} \]

\[ \text{RBW} = 100 \text{ kHz}, \text{VBW} = 1 \text{ kHz} \]

\[ -106 \text{ dBc/Hz @ 3 MHz} \]
25.9-GHz VCO

Measurement result -- frequency tuning range

- Non-monotonic tuning characteristic
- ~600 MHz frequency tuning range
  + Small varactor capacitance range
  + Partially scaled design rules
- Phase noise flatness: 1 dB
25.9-GHz VCO

- Die Area: 486 x 511 µm²
- Diamond-shape pads for reduced pad capacitance
- Ground-shielded pads (p⁺-diffusion instead of polysilicon ground shield for reducing pad capacitance)
## 25.9-GHz VCO

### Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.1 μm (L_{poly}) Bulk CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Resistivity</td>
<td>~1 Ω-cm</td>
</tr>
<tr>
<td>SSB Phase Noise when ( f_0 = 25.9 ) GHz (dBc/Hz @ offset)</td>
<td>-96 @ 1 MHz, -106 @ 3 MHz</td>
</tr>
<tr>
<td>Tuning Range (GHz/V_{ctl})</td>
<td>600 MHz ((25.3/0.7 - 25.9/1.5))</td>
</tr>
<tr>
<td>Phase Noise Flatness</td>
<td>1 dB</td>
</tr>
<tr>
<td>Output Power Flatness</td>
<td>1.5 dB</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>24 mW (16 mA @ 1.5 V)</td>
</tr>
<tr>
<td>Inductor Q</td>
<td>~3 @ 26 GHz</td>
</tr>
<tr>
<td>Varactor Q</td>
<td>&gt;20 @ 26 GHz</td>
</tr>
<tr>
<td>Die Area</td>
<td>486 x 511 μm²</td>
</tr>
</tbody>
</table>

- A fully functional CMOS VCO has been demonstrated operating at >25 GHz
- MOS varactor Q of >20 at 26 GHz has been measured
- Effects of polysilicon depletion on VCO tuning characteristic was investigated
Conclusions

• Low-cost and easy-to-implemented passive components were presented with high quality factors suitable for most applications

• 1 and 5.5-GHz LC VCOs were demonstrated with excellent phase noise performance, and reasonable tuning range and current consumption

• A CMOS LC VCO operating at ~26 GHz was demonstrated which is currently the CMOS circuit with the highest operating frequency suggesting that fully-scaled advanced CMOS technologies are capable of >30-GHz applications