

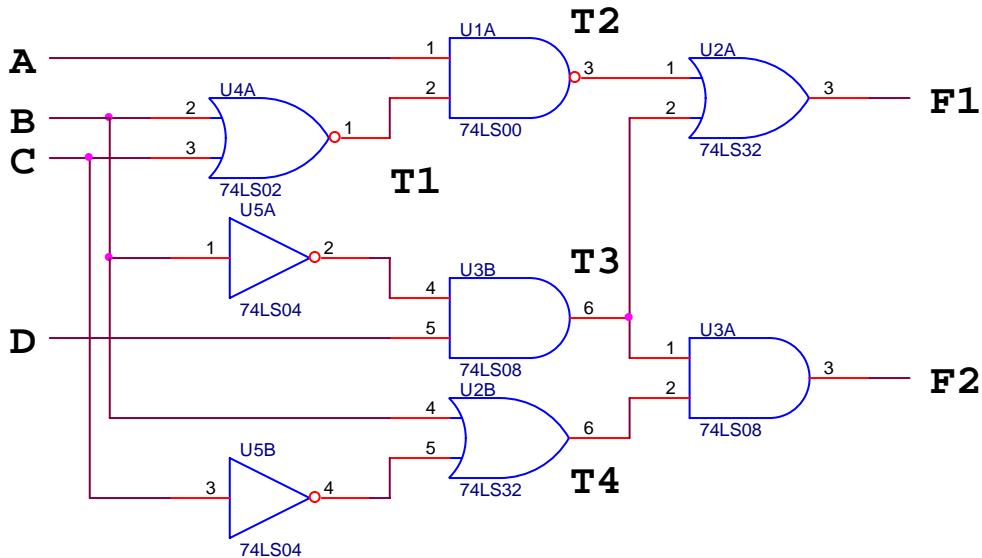
## EE 2381 DIGITAL COMPUTER LOGIC

**Homework #5**  
**13 Feb 2007**

**Professor Jim Dunham**  
**Due: 27 Feb 2007**

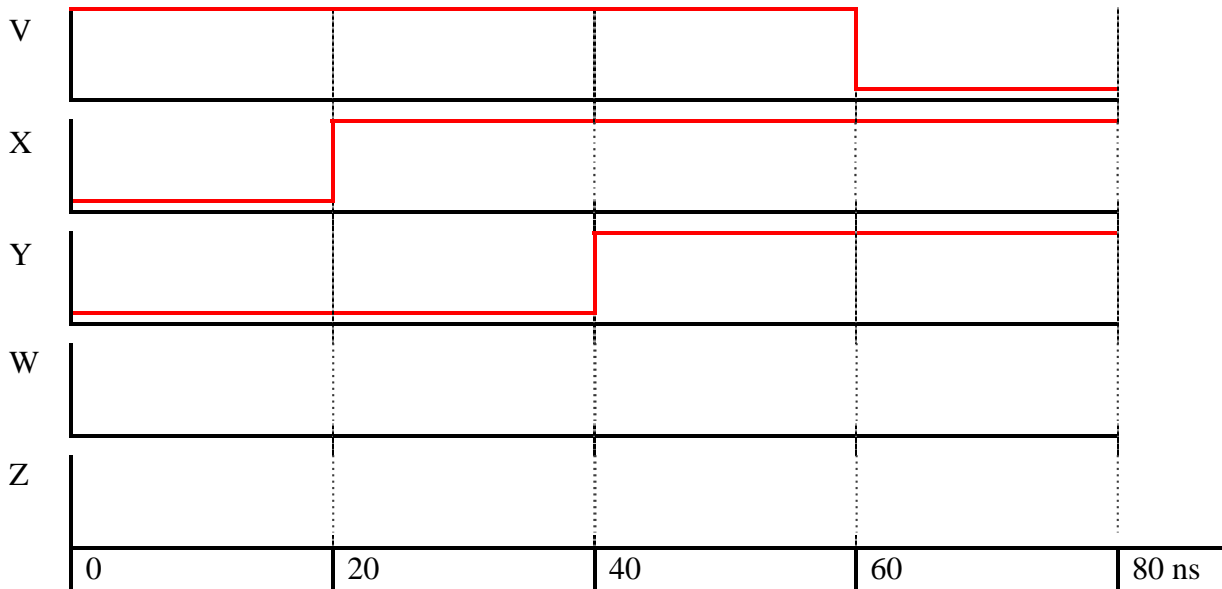
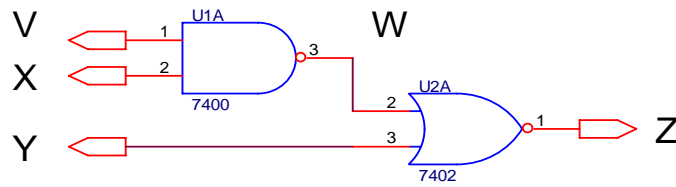
Review Text: Chapter 4, sections 1-3, 8, 10 & 11 (skim three-state gate materials).

1. Consider the combinational circuit shown in the figure below:



- a. Derive the Boolean expressions for  $T_1$  through  $T_4$ . Evaluate the outputs  $F_1$  and  $F_2$  as functions of the four inputs.
- b. List the truth table with 16 binary combinations of the four input variables. Then list the binary values for  $T_1$  through  $T_4$  and outputs  $F_1$  and  $F_2$  in the table.
- c. Plot the output Boolean function obtained in part (b) on maps and show that the simplified Boolean expressions are equivalent to the ones obtained in part (a).

2. Provide a timing diagram for the network shown below from time 0 to time 80 ns. Assume that both NAND and OR gates have a propagation delay of 5 ns.



3. Complete the timing diagram for the circuit below under the following assumptions:
- NAND and NOR gate rise time delay is 10 ns and fall time delay is 5 ns;
  - NOT gate rise time delay is 15 ns and fall time delay is 10 ns;
  - OR gate rise time delay is 5 ns and fall time delay is 10 ns; and
  - All gates are initially in an *unknown state*. If you have problems, assume steady-state values and continue with the rest of the problem.

