

EE 2381 DIGITAL COMPUTER LOGIC

Homework #8
20 Mar 2007

Professor Jim Dunham
Due: 27 Mar 2007

Review Text: Chapter 5, sections 1-3 and 7 (focus on excitation tables and maps for flip-flop inputs).

1. Mano 5-1. Use Verilog to verify your circuits operation.
2. Mano 5-3.
3. Assume the following operations and values for a flip-flop with the inputs P and N :

Operation	PN
No Change	10
Clear to 0	00
Set to 1	11
Complement	01

- a. Tabulate the characteristic table
 - b. Derive the characteristic equation
 - c. Tabulate the excitation table
 - d. Show how this flip-flop can be converted to a D flip-flop.
4. Design a counter which counts in the following sequence: 000, 011, 101, 100, 111, 000, ...
 - a. Use positive edge-triggered D flip-flops and NAND gates.
 - b. Use negative edge-triggered J-K flip-flops and NOR gates.