

EE 2381 DIGITAL COMPUTER LOGIC

Homework #11
12 Apr 2007

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Due: 19 Apr 2007

Review Text: Chapter 6.

1. Mano 6-3.
2. Mano 6-4. Assume that the contents of the register is 1011 and the input sequence is 011100.
3. Mano 6-8. Assume that the content of Register A is 0110 and the content of Register B is 0101.
4. Mano 6-15. Assume that all flip-flops have a 3.3 ns delay (74F family of logic).
5. How many flip-flops will be complemented in a 8-bit binary ripple counter to reach the next count after the following count:
 - (a) 11011111
 - (b) 10101011
 - (c) 11001111.
6. Consider the 4-bit binary counter with parallel load shown in Figure 6-14 of Mano. Construct a counter that counts from 0000 to 1010. *Hint:* Take advantage of the load feature.
7. A Moore sequential network has one input and one output. When the input sequence 101 occurs, the output becomes 1 and remains 1 until the sequence 101 occurs again at which time the output returns to 0. The output then remains 0 until 101 occurs a third time, *etc.* Thus the output is complemented every time the sequence 101 occurs. Derive the state graph and demonstrate that your solution is optimal in the sense of having a minimum number of states. Assume initially that no inputs have been seen.
8. In a feedback shift register circuit, a function of the shift register's state (the outputs Q_A , Q_B , Q_C and Q_D) is feed back into the input of the shift register. For the feedback shift register circuit below, indicate the shift register's state for the first four clock pulses given the initial state of all zeros. *Hint:* Exploit the behavior of a shift register to simplify your work.

