

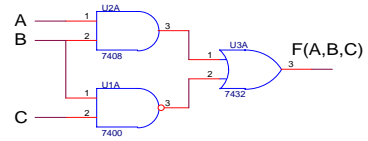
# EE 2381 DIGITAL COMPUTER LOGIC

## Introduction and Overview:

- Analysis and Design
- Combinational and Sequential Circuits
- Simulation vs Hardware

## Goal: Analysis and synthesis of combinational network:

$$f(A, B, C) = AB + (BC)'$$



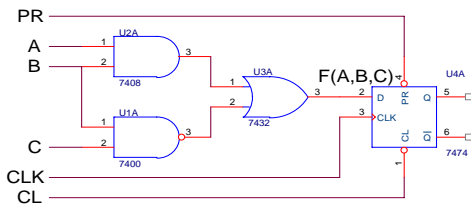
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## Goal: Analysis and synthesis of sequential network

$$f(A, B, C) = AB + (BC)'$$



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```

module MAIN;                                     // Combinational Network Simulation
  reg A,B,C;
  wire D,E,F;

  and #(17,12) u01A(D,A,B); // AND gates
  nand #(11,07) u02A(E,B,C); // NAND gate
  or #(10,14) u03A(F,D,E); // OR gate

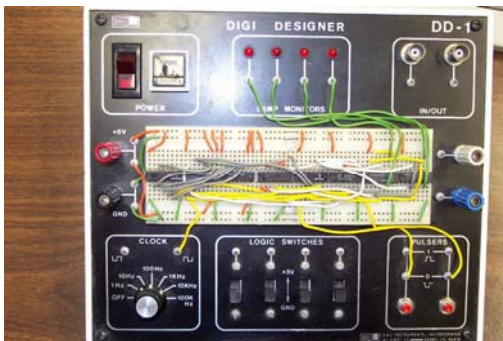
  initial
  begin
    $monitor($time, " - A=%b B=%b C=%b D=%b E=%b F=%b",A,B,C,D,E,F);
    #100 A=0;B=0;C=0;
    #100 A=0;B=0;C=1;
    #100 A=0;B=1;C=0;
    #100 A=0;B=1;C=1;
    #100 A=1;B=0;C=0;
    #100 A=1;B=0;C=1;
    #100 A=1;B=1;C=0;
    #100 A=1;B=1;C=1;
    #100 $finish;
  end
endmodule

```

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