

Integrated Circuit (IC)

- Several Terms
 - Fan-out
 - Specify the number of standard loads that the output of the typical gates can drive without impairing its normal operation.
 - Fan-in
 - The number of inputs available in a gate
 - Power dissipation
 - Power consumed by the gate that must be available from the power supply.
 - Propagation delay
 - The average transition delay time for a signal to propagate from input to output
 - Noise margin
 - The Maximum external noise voltage added to an input signal that does not cause an undesirable change in the circuit output

Compute-Aided Design (CAD)

- or Electrical Design Automation (EDA)
 - Design is too large to be handled manually
 - Different level of tools exist
 - FloorPlan, Placement and Route
 - Synthesis
 - Simulation
 - Hardware Description language
 - Verilog
 - VHDL
 - System Verilog
 - Different between software and hardware

HARDWARE DESCRIPTION LANGUAGES (HDLs)

- Textual Representation of Digital Circuit
 - Yet Another Way (truth tables, equations, circuit diagrams, etc.)
- Why Have HDLs?
 - Documentation
 - First common HDL (VHDL) Documentation Language
 - Simulation
 - First common HDL for Simulation (Verilog)
 - Synthesis
 - Both VHDL and Verilog used for this
 - Currently, more emphasis on SystemC, SystemVerilog

HARDWARE DESCRIPTION LANGUAGES (HDLs)

- Why are HDLs Important?
 - Easy way to Describe Large Circuits
 - Large Teams of Designers can Work Concurrently Using Software Engineering Techniques
 - The Specification can be Simulated
 - The Specification can be Synthesized
 - HDLs Support Multiple Levels of Abstraction

Definitions

- Specification
 - Description of the Desired Functionality
- Simulation
 - Given a Model and Inputs, Predict the Output
- Synthesis
 - Transform One Model into Another

Why Another Language?

- Sequential Languages
 - Programming Languages are *Sequential*
 - Each Statement is Executed in Order of Appearance
- Hardware is a Parallel Instance
 - Model in Terms of *Events*
 - More Natural Way to Describe and *Simulate*
- HDLs can be tricky because:
 - We are used to *Sequential Execution*
 - Different “bugs” Occur due to *Parallel Behavior*
 - Parallel Behavior Modeled Using *Event Driven* Methods