

# Tutorial for Cadence SimVision Verilog Simulator Tool

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## Contents

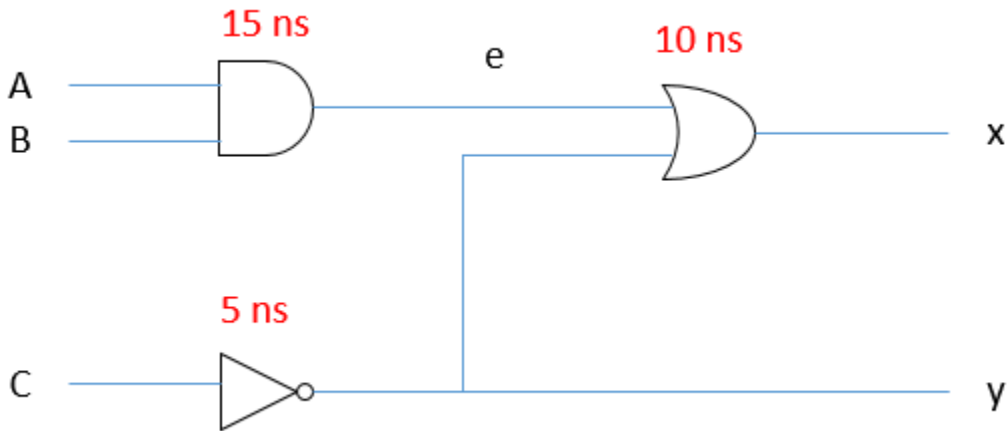
- 1 Overview ..... 1
- 2 Preliminary Setup..... 1
  - 2.1 Program Code for ex3.v ..... 2
  - 2.2 Program Code for ex3\_tb\_wave.v ..... 3
- 3 Starting SimVision Tool and Reading in the Verilog files ..... 4
- 4 View Waveforms ..... 5
  - 4.1 Setup ..... 5
  - 4.2 Waveform Viewer ..... 6
- 5 Exiting the Tool ..... 8

## 1 Overview

The SimVision simulator tool can show waveforms for Verilog code. These waveforms help identify circuit delays and other timing issues in Verilog circuits.

## 2 Preliminary Setup

The example code simulates the behavior of a simple logic circuit, shown below. Note that each logic gate has a delay value indicated in nanoseconds (ns).



You will use the following Verilog files for your simulation example:

1. ex3.v: Verilog code for simple logic circuit
2. ex3\_tb\_wave.v: testbench code to test logic circuit and generate waveforms
  - a. NOTE: the testbench has a 50 ns clock period (clock rate = 20 MHz). The inputs to the testbench module will update every clock period (DELAY value)

## 2.1 Program Code for ex3.v

```
// ex3.v
// T. Manikas 2022 Jan 12
// simple structural circuit with delay
// add timescale of 1 ns
// modify gate delays

`timescale 1ns/10ps

// Description of circuit with delay
module circuit_with_delay (A,B,C,x,y);
    input A,B,C;
    output x,y;
    wire e;
    and #(15) g1(e,A,B);
    not #(5) g2(y,C);
    or #(10) g3(x,e,y);
endmodule
```

## 2.2 Program Code for ex3\_tb\_wave.v

```
// ex3_tb_wave.v
// T. Manikas 2022 Jan 13
// testbench for ex1.v module
// add timescale of 1 ns
// display waveform for output

`timescale 1ns/10ps
`define DELAY 50

// Stimulus for simple circuit
module stimcrct;

    parameter finishtime = 5;

    reg A, B, C;
    wire x, y;
    circuit_with_delay cwd (A, B, C, x, y);

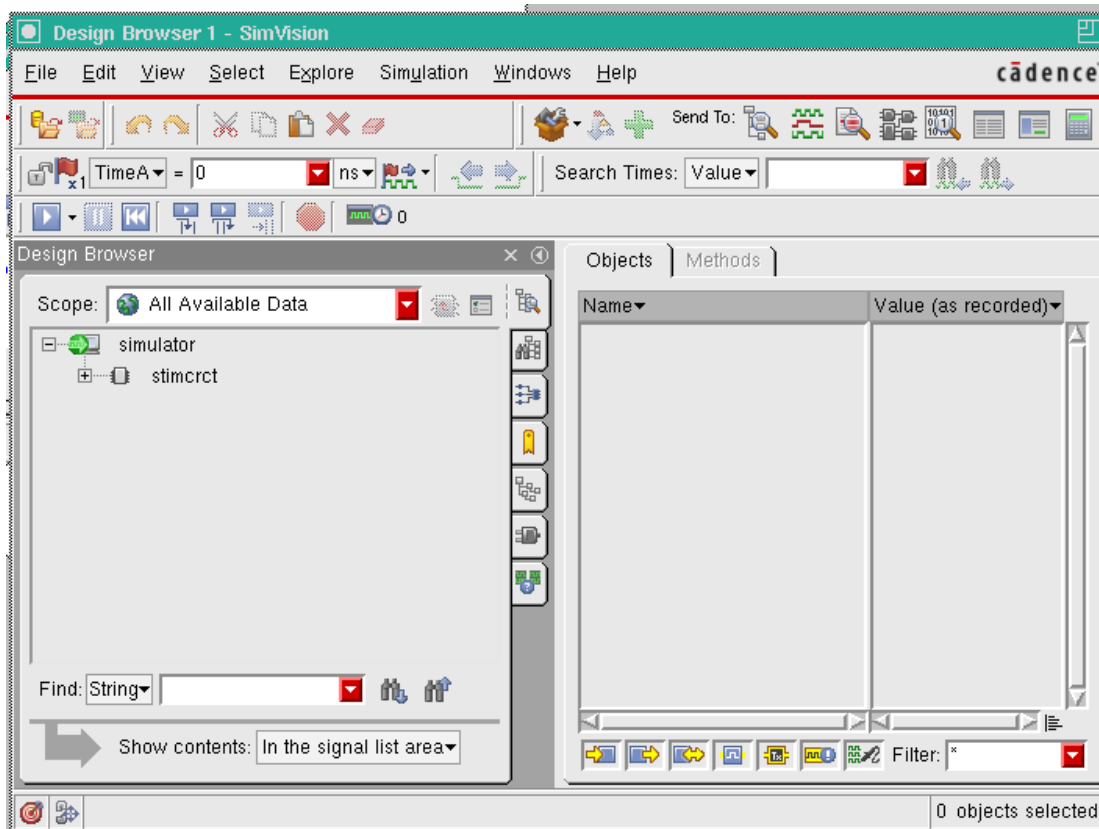
    initial begin
        #0 A=1'b0; B=1'b0; C=1'b0;
        #`DELAY
        C=1'b1;
        #`DELAY
        B=1'b1;
        #`DELAY
        A=1'b1;
        $stop;
    end

    initial begin
        $monitor($time, " A=%b B=%b C=%b x=%b y=%b",A,B,C,x,y);
    end

endmodule
```

### 3 Starting SimVision Tool and Reading in the Verilog files

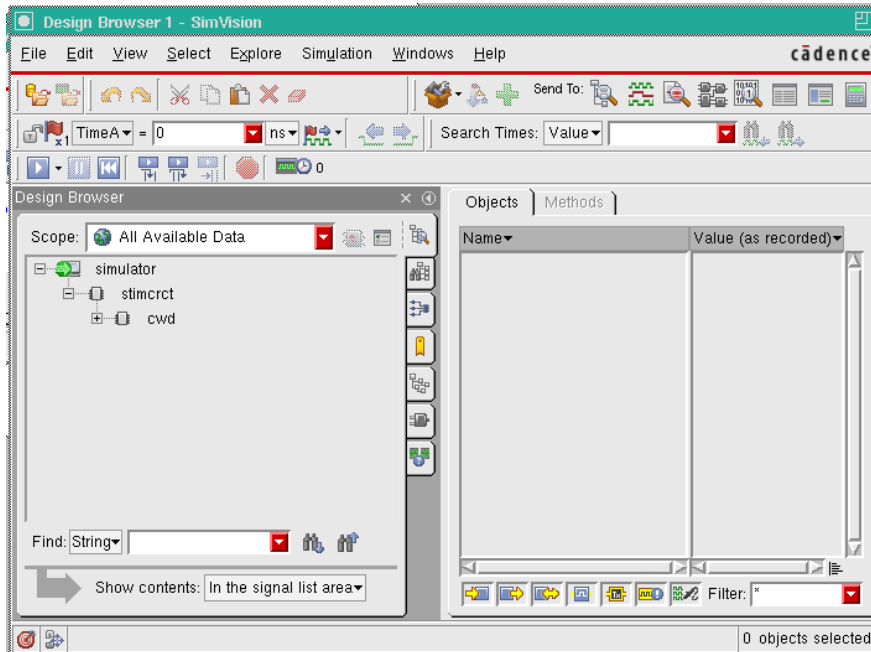
1. At the Unix prompt, type the following command:  
**xmverilog -gui -access +rw ex3.v ex3\_tb\_wave.v &**
2. If there are no errors, two windows will pop up: **Console** and **Design Browser 1**.
3. However, if there **are** errors, the tool will display the error messages and will not launch these windows. Usually, errors are due to typos in your Verilog file – please correct the errors using your text editor, then try to run SimVision again.



## 4 View Waveforms

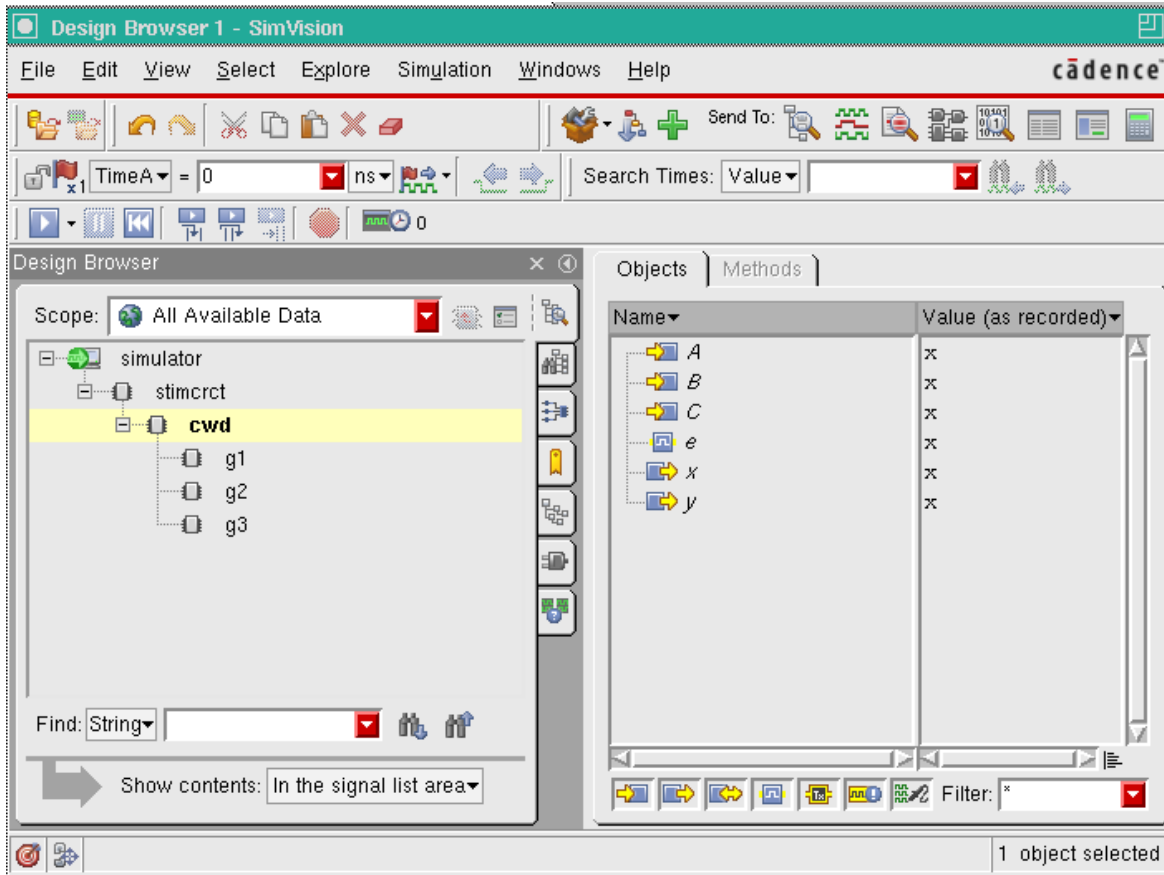
### 4.1 Setup

1. In the Design Browser Window, click on "+" next to **stimcrct**. This will cause **cwd** to be displayed under **stimcrct**.



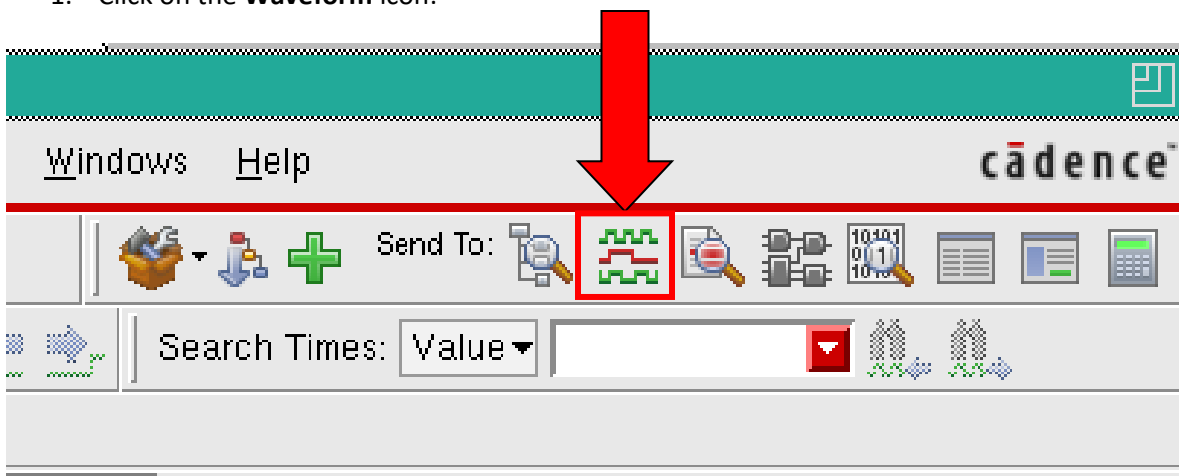
2. Click on "+" next to **cwd**. This will display **g1**, **g2**, and **g3**.

- Click on **cwd**. This will display all signals (A,B,C,e,x,y) to be displayed in the **Objects** area.

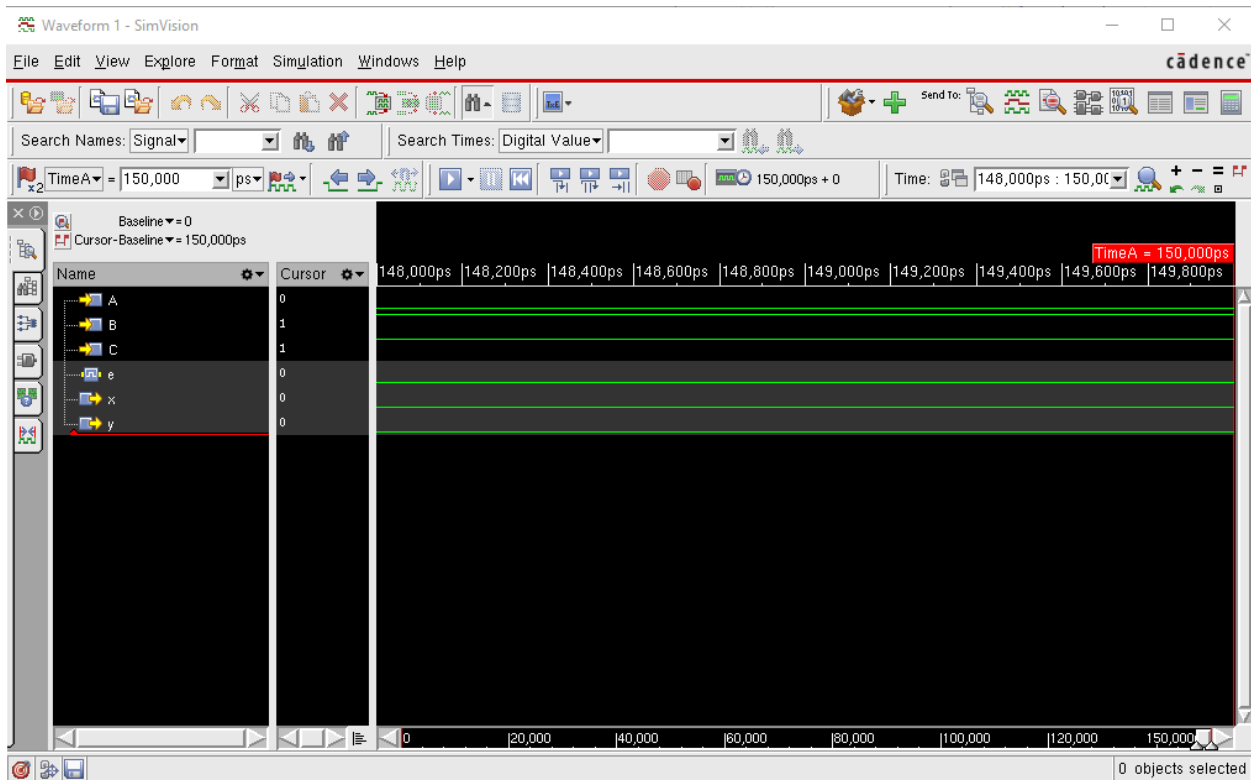
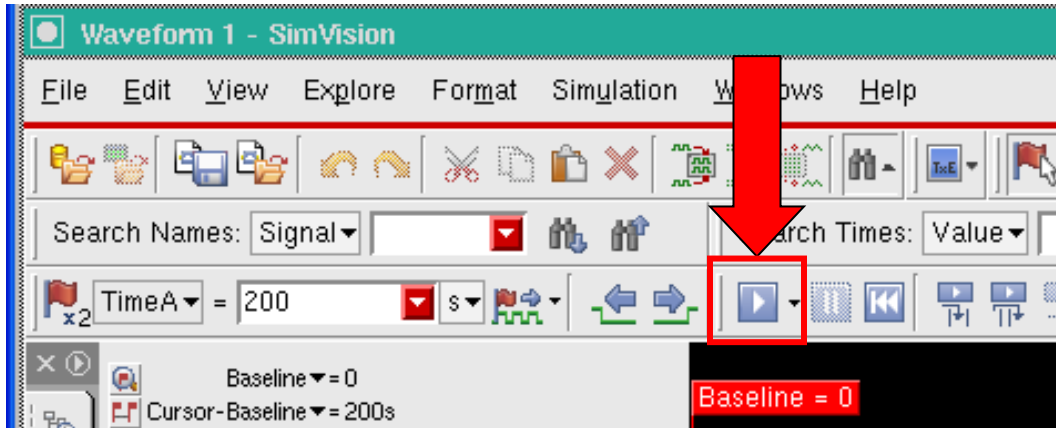


## 4.2 Waveform Viewer

- Click on the **Waveform** icon:



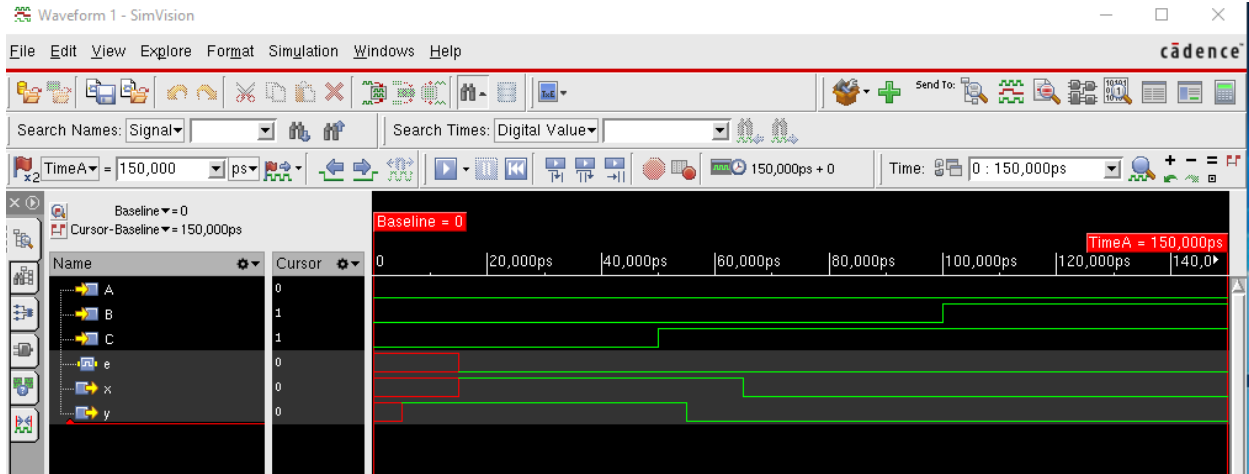
- This will open the **Waveform** window. Click on the **Run** icon to generate the signal waveforms for our example Verilog circuit:



- To scale the waveforms so that you can see the results, use the **“Zoom out fully on x-axis”** icon. This looks like an equals (=) sign.



4. This will give you the following waveforms. Note that output signals **x** and **y** are red lines at the beginning of the simulation. Due to delays through the logic gates, the logic values of signals **x** and **y** are initially undefined.
  - a. Also note the effects of the gate delays. For example, when input C switches from 0 to 1, there is a 5 ns delay (inverter) before output **y** switches from 1 to 0.



## 5 Exiting the Tool

To exit the tool, use the pulldown menu on any of these windows and select **File, Exit SimVision**.