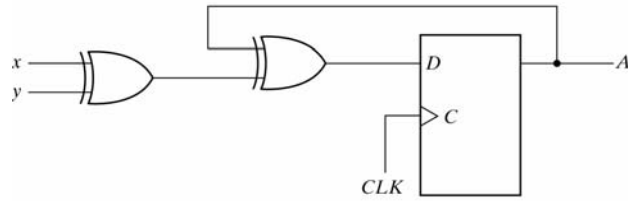


## D-Flip-flop Synchronous Circuit

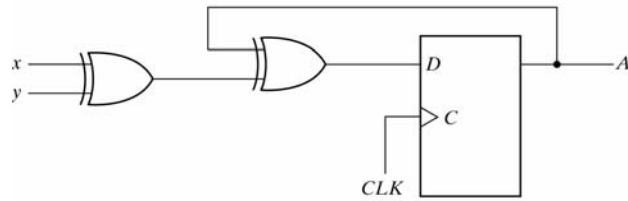


(a) Circuit diagram

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Fig. 5-17 Sequential Circuit with *D* Flip-Flop

## D-Flip-flop Synchronous Circuit



(a) Circuit diagram

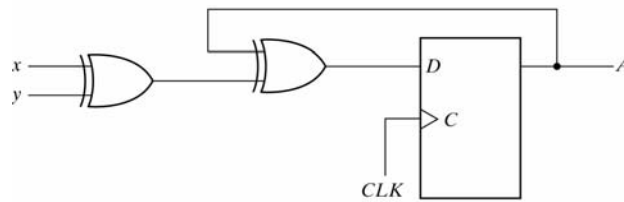
$$A(t+1) = D$$

$$D = A(t) \oplus x \oplus y$$

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Fig. 5-17 Sequential Circuit with *D* Flip-Flop

## D-Flip-flop Synchronous Circuit



(a) Circuit diagram

Present state	Inputs		Next state
<i>A</i>	<i>x</i>	<i>y</i>	<i>A</i>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table

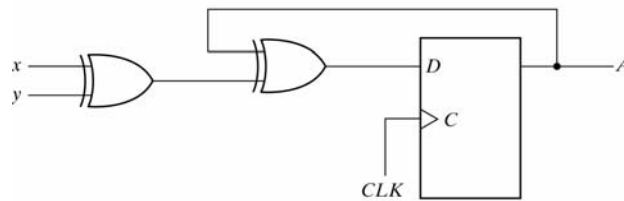
$$A(t+1) = D$$

$$D = A(t) \oplus x \oplus y$$

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Fig. 5-17 Sequential Circuit with *D* Flip-Flop

## D-Flip-flop Synchronous Circuit



(a) Circuit diagram

Present state	Inputs		Next state
<i>A</i>	<i>x</i>	<i>y</i>	<i>A</i>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table

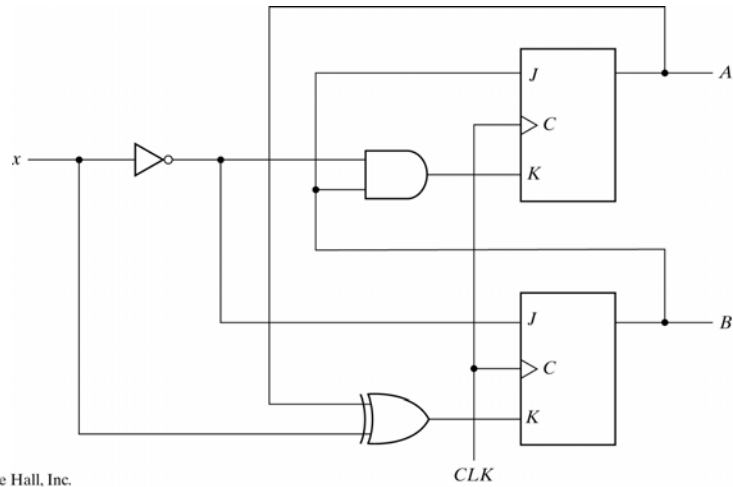


(c) State diagram

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Fig. 5-17 Sequential Circuit with *D* Flip-Flop

## JK-Flip-flop Synchronous Circuit



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Fig. 5-18 Sequential Circuit with JK Flip-Flop

## JK-Flip-flop Synchronous Circuit

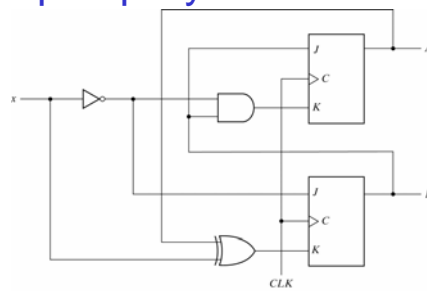


Fig. 5-18 Sequential Circuit with JK Flip-Flop

$$A(t+1) = J_A \bar{A}(t) + \bar{K}_A A(t)$$

$$B(t+1) = J_B \bar{B}(t) + \bar{K}_B B(t)$$

$$J_A = B(t) \quad K_A = \bar{x}B(t)$$

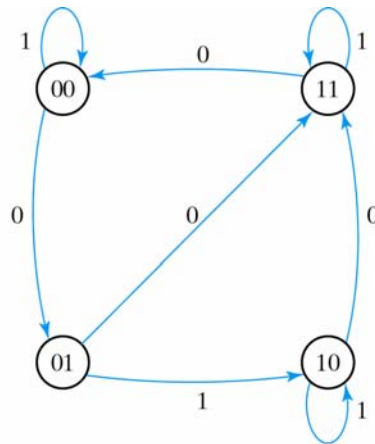
$$J_B = \bar{x} \quad K_B = A(t) \oplus x$$

$$A(t+1) = \bar{A}(t)B(t) + \overline{(\bar{x}B(t))}A(t)$$

$$B(t+1) = \bar{x}\bar{B}(t) + \overline{(A(t) \oplus x)}B(t)$$

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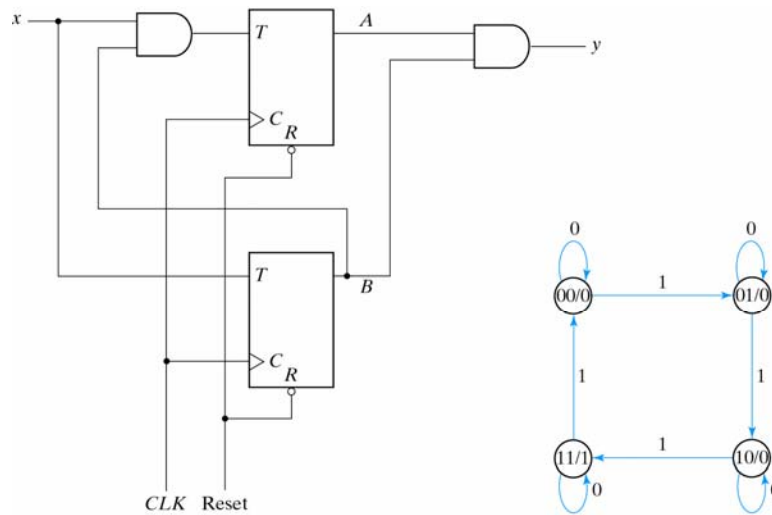
## JK-Flip-flop Circuit State Diagram



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Fig. 5-19 State Diagram of the Circuit of Fig. 5-18

## T-Flip-flop Synchronous Circuit



(a) Circuit diagram

(b) State diagram

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Fig. 5-20 Sequential Circuit with *T* Flip-Flops

## State Reduction and Assignment

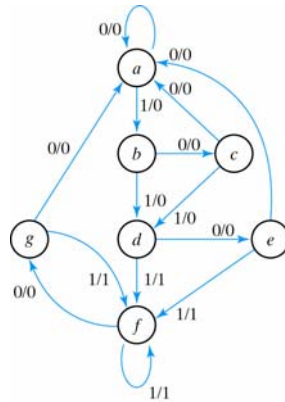


Fig. 5-22 State Diagram

state	<i>a</i>	<i>a</i>	<i>b</i>	<i>c</i>	<i>d</i>	<i>e</i>	<i>f</i>	<i>f</i>	<i>g</i>	<i>f</i>	<i>g</i>	<i>a</i>
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

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## State Reduction Procedure

1. Form the State Table
2. Two States are Equivalent if, for each member of the set of inputs, they give the same output and transition to the same state
3. For equivalent states, remove one and relabel the removed state with the equivalent

## State Table

Present State	Next State		Output	
	<i>x</i> =0	<i>x</i> =1	<i>x</i> =0	<i>x</i> =1
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	<i>f</i>	0	1
<i>e</i>	<i>a</i>	<i>f</i>	0	1
<i>f</i>	<i>g</i>	<i>f</i>	0	1
<i>g</i>	<i>a</i>	<i>f</i>	0	1

## Reducing the State Table

Present State	Next State		Output	
	<i>x</i> =0	<i>x</i> =1	<i>x</i> =0	<i>x</i> =1
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	<i>f</i>	0	1
<i>e</i>	<i>a</i>	<i>f</i>	0	1
<i>f</i>	<i>e</i>	<i>f</i>	0	1

## Reduced State Table

Present State	Next State		Output	
	x=0	x=1	x=0	x=1
<i>a</i>	<i>a</i>	<i>b</i>	0	0
<i>b</i>	<i>c</i>	<i>d</i>	0	0
<i>c</i>	<i>a</i>	<i>d</i>	0	0
<i>d</i>	<i>e</i>	<i>d</i>	0	1
<i>e</i>	<i>a</i>	<i>d</i>	0	1

## Reduced State Diagram

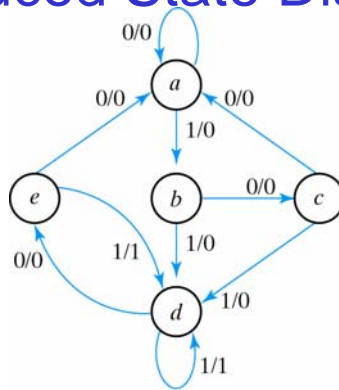


Fig. 5-23 Reduced State Diagram

state	<i>a</i>	<i>a</i>	<i>b</i>	<i>c</i>	<i>d</i>	<i>e</i>	<i>d</i>	<i>d</i>	<i>e</i>	<i>d</i>	<i>e</i>	<i>a</i>
input	0	1	0	1	0	1	1	0	1	0	0	
output	0	0	0	0	0	1	1	0	1	0	0	

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## State Assignment

1. Must Assign a unique bit pattern to each state to design a circuit
2. Minimum number of bits required is  $\lceil \log_2(m) \rceil$  for  $m$  states
3. Can use Binary Encoding, Gray Code, etc.
4. One-hot Encoding uses  $m$  bits
5. State Assignment Can affect Your Circuit
  1. Area
  2. Speed
  3. Functionality

## Reduced State Table State Assignment Possibilities

State	Assignment 1 Binary	Assignment 2 Gray Code	Assignment 3 One-hot
<i>a</i>	000	000	00001
<i>b</i>	001	001	00010
<i>c</i>	010	011	00100
<i>d</i>	011	010	01000
<i>e</i>	100	110	10000

## Reduced State Table with Binary Assignment

<b>Present State</b>	<b>Next State</b>		<b>Output</b>	
	$x=0$	$x=1$	$x=0$	$x=1$
000	000	001	0	0
001	010	011	0	0
010	000	011	0	0
011	100	011	0	1
100	000	011	0	1

## Design Procedure

1. Derive the state diagram for the circuit
2. Reduce the number of states
3. Assign binary values to the states
4. Obtain binary-coded state table
5. Choose the type of FFs to be used
6. Derive the simplified FF input equations and output equations
7. Draw the logic diagram

## Design Example

1. Derive the state diagram for the circuit

*Design a circuit that detects three or more consecutive 1's in a string of bits coming through an input line*

## Design Example

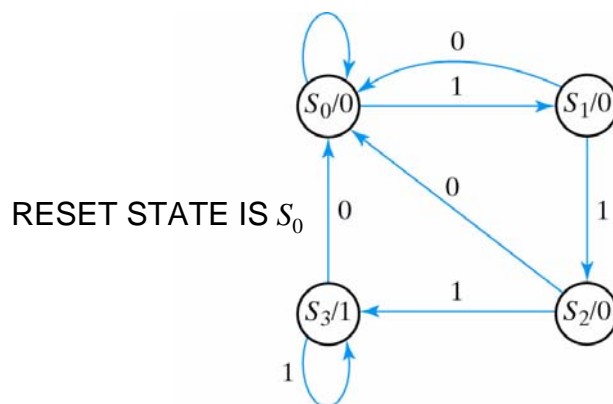


Fig. 5-24 State Diagram for Sequence Detector

## State Table with Binary Assignment

Present State		Input	Next State		Output
A	B	x	A	B	y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

## Design Example

5. Choose the type of FFs to be used

*Choose D-Flip-flops*

From Table, the Excitation Equations are:

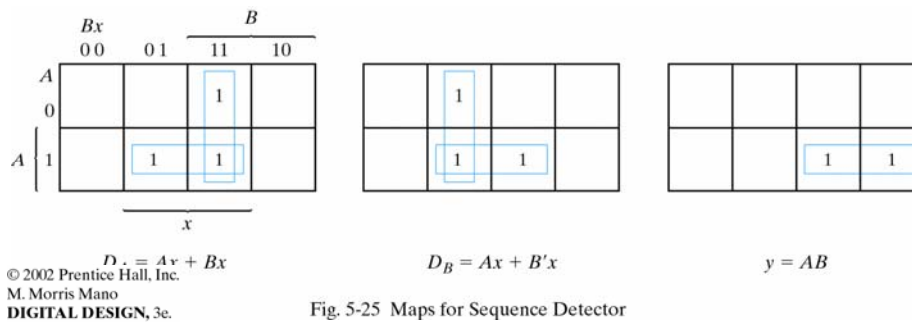
$$A(t+1) = D_A(A, B, x) = \sum(3, 5, 7)$$

$$B(t+1) = D_B(A, B, x) = \sum(1, 5, 7)$$

$$y(A, B, x) = \sum(6, 7)$$

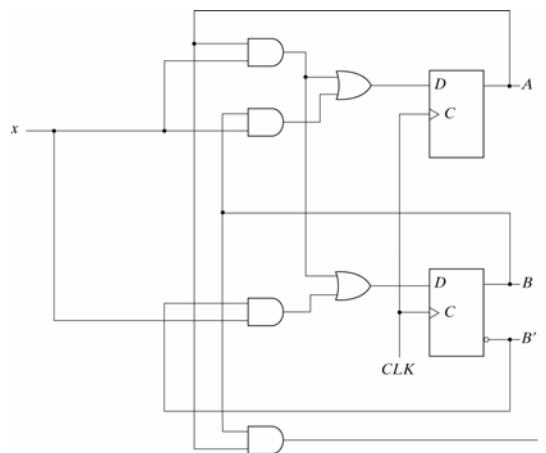
## Design Example

6. Derive the simplified FF input equations and output equations



## Design Example

7. Draw the logic diagram



## Excitation Tables

- If D-FFs Used, excitation equations taken directly from the State Table
- Not the Case for JK and T flip-flops
- Excitation Equations Derived Indirectly from State Table
- Useful to Use FF Excitation Tables
- Same Information in Characteristic Tables but in a Different Form

## Excitation Tables

$Q(t)$	$Q(t+1)$	$J$	$K$
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$Q(t)$	$Q(t+1)$	$T$
0	0	0
0	1	1
1	0	1
1	1	0

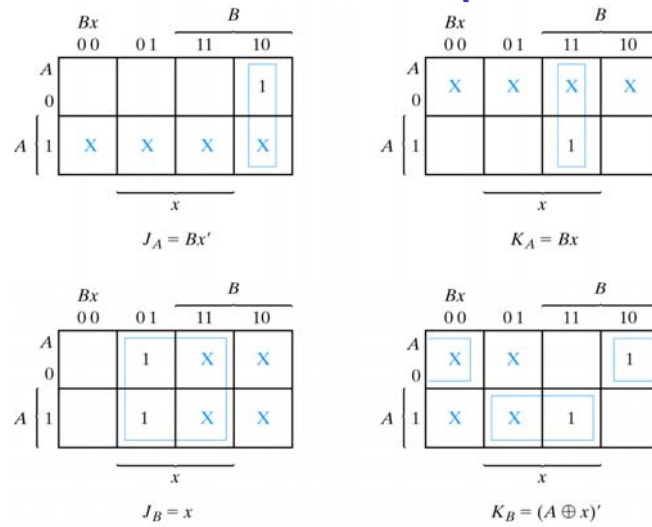
## State Table Example with JK FFs

Present State		Input	Next State		Flip-Flop Inputs			
A	B		A	B	$J_A$	$K_A$	$J_B$	$K_B$
0	0	0	0	0				
0	0	1	0	1				
0	1	0	1	0				
0	1	1	0	1				
1	0	0	1	0				
1	0	1	1	1				
1	1	0	1	1				
1	1	1	0	0				

## State Table Example with JK FFs

Present State		Input	Next State		Flip-Flop Inputs			
A	B		A	B	$J_A$	$K_A$	$J_B$	$K_B$
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	1	0	1	X	X	1
0	1	1	0	1	0	X	X	0
1	0	0	1	0	X	0	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	X	1	X	1

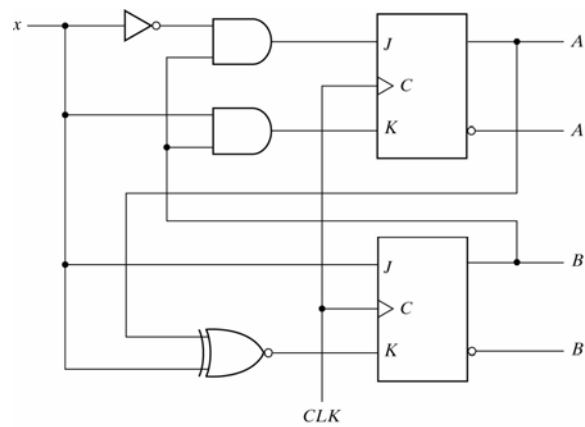
# JK-FF Excitation Equations



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Fig. 5-27 Maps for J and K Input Equations

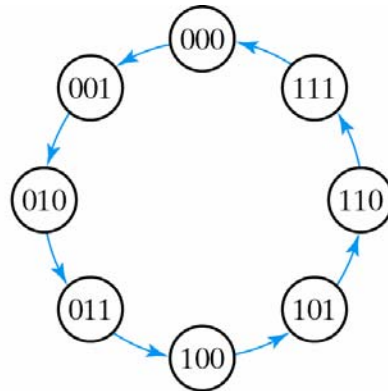
# JK-FF Logic Diagram



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Fig. 5-28 Logic Diagram for Sequential Circuit with JK Flip-Flops

## Design Example with T-FFs



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Fig. 5-29 State Diagram of 3-Bit Binary Counter

## 3-bit Counter Example with T-FFs

Present State			Next State			Flip-flop Inputs		
$A_2$	$A_1$	$A_0$	$A_2$	$A_1$	$A_0$	$T_{A2}$	$T_{A1}$	$T_{A0}$
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

## T-FF Excitation Equations

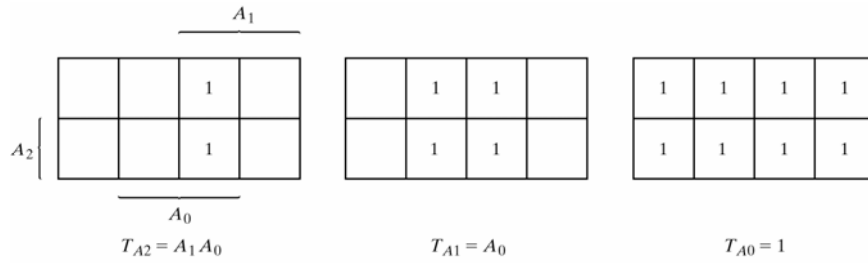


Fig. 5-30 Maps for 3-Bit Binary Counter

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## 3-bit Counter with T-FFs

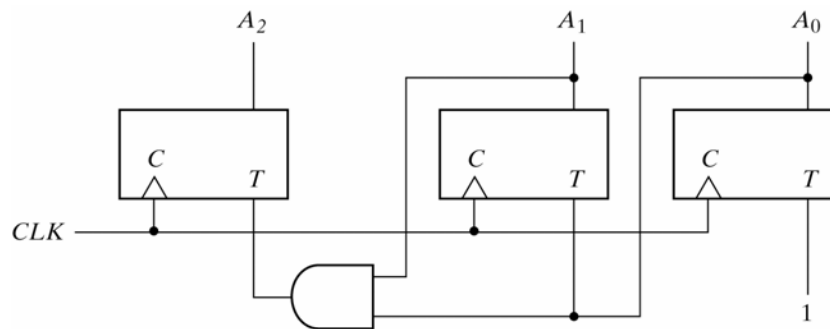


Fig. 5-31 Logic Diagram of 3-Bit Binary Counter

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## Design Example

*Design a selectable 2-bit binary  
up/down counter*