

SEQUENTIAL LOGIC

- Feedback from Storage Elements into CL
- “State” Content of Storage Elements at any Given Time Instant

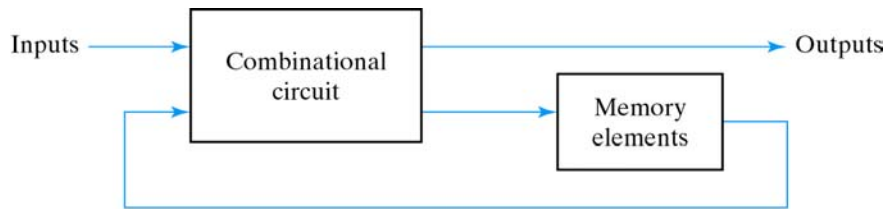
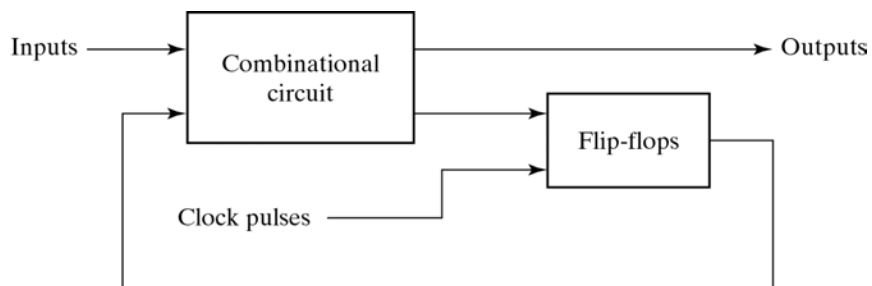


Fig. 5-1 Block Diagram of Sequential Circuit

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SYNCHRONOUS SEQUENTIAL LOGIC



(a) Block diagram



(b) Timing diagram of clock pulses

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Fig. 5-2 Synchronous Clocked Sequential Circuit

Set-Reset Latch

- Must Use Delays in this Analysis
- Basic Storage Element – Level Sensitive



Fig. 5-3 SR Latch with NOR Gates

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Set-Reset Latch

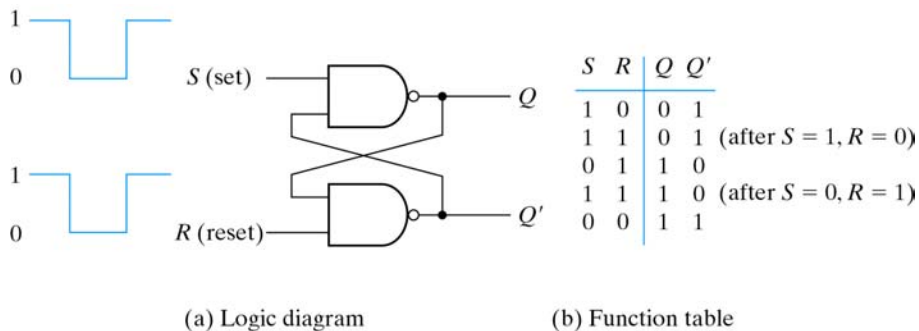
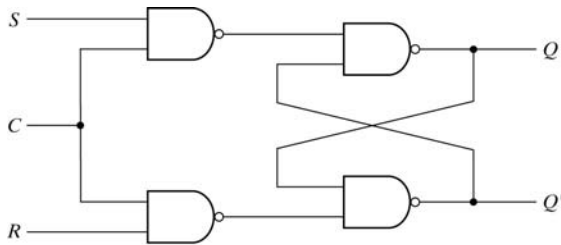


Fig. 5-4 SR Latch with NAND Gates

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SR Latch with Control Input



(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	$Q = 0$; Reset state
1	1	0	$Q = 1$; set state
1	1	1	Indeterminate

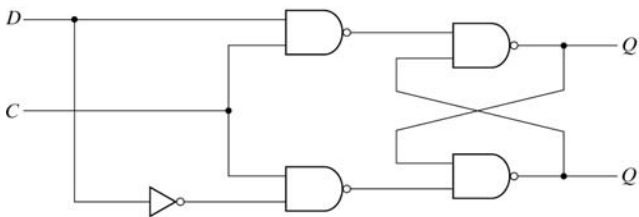
(b) Function table

Fig. 5-5 SR Latch with Control Input

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Data (D) Latch

Avoids Indeterminate State of SR Latch



(a) Logic diagram

C	D	Next state of Q
0	X	No change
1	0	$Q = 0$; Reset state
1	1	$Q = 1$; Set state

(b) Function table

Fig. 5-6 D Latch

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GRAPHIC SYMBOLS FOR LATCHES

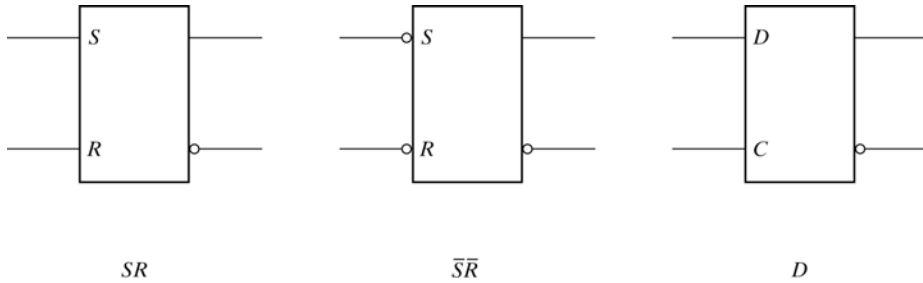


Fig. 5-7 Graphic Symbols for Latches

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LEVEL vs. EDGE-SENSITIVE



(a) Response to positive level



(b) Positive-edge response



(c) Negative-edge response

Fig. 5-8 Clock Response in Latch and Flip-Flop

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EDGE-TRIGGERED *D* FLIP-FLOP

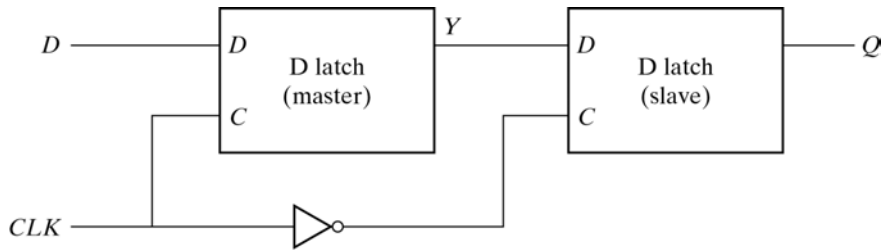
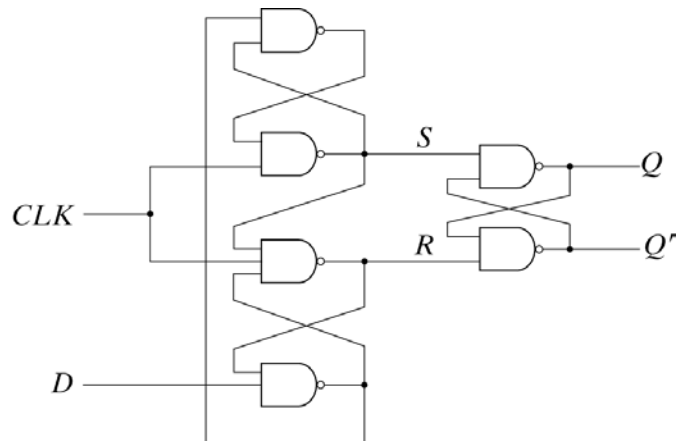


Fig. 5-9 Master-Slave *D* Flip-Flop

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EDGE-TRIGGERED *D* FLIP-FLOP

More Efficient Implementation of a D Flip-Flop

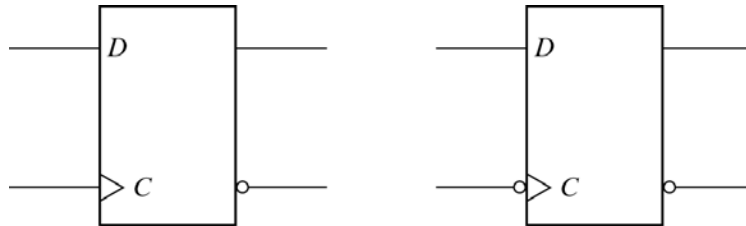


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Fig. 5-10 *D*-Type Positive-Edge-Triggered Flip-Flop

D FLIP-FLOPS

Most Common Edge-triggered Device in Use



(a) Positive-edge

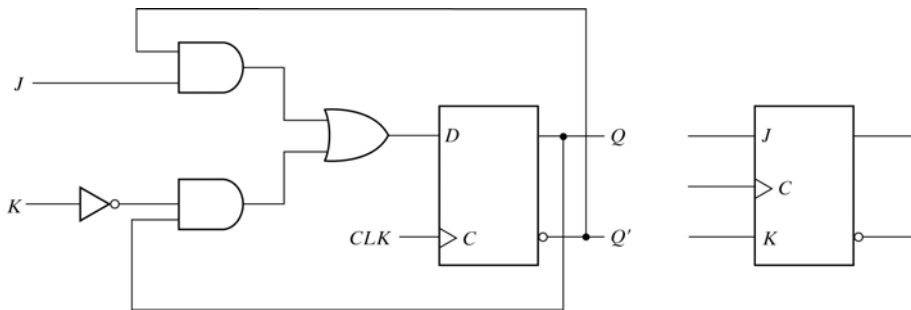
(a) Negative-edge

Fig. 5-11 Graphic Symbol for Edge-Triggered *D* Flip-Flop

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JK FLIP-FLOPS

$$D = J\bar{Q} + \bar{K}Q$$



(a) Circuit diagram

(b) Graphic symbol

Fig. 5-12 *JK* Flip-Flop

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Toggle (T) FLIP-FLOPS

$$D = T \oplus Q = T\bar{Q} + \bar{T}Q$$

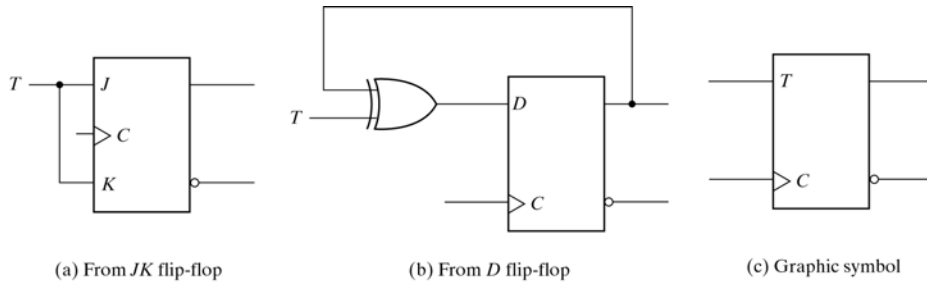


Fig. 5-13 T Flip-Flop

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Characteristic Tables

- Describes FF Operation in Tabular Form
- Useful for Analysis of FF Circuits

JK Flip-Flop			
J	K	$Q(t+1)$	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}(t)$	Complement

D Flip-Flop		
D	$Q(t+1)$	
0	0	Reset
1	1	Set

T Flip-Flop		
T	$Q(t+1)$	
0	$Q(t)$	Reset
1	$\bar{Q}(t)$	Set

Characteristic Equations

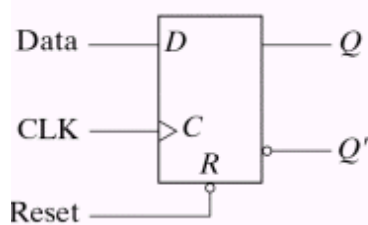
- Describes FF Operation in Equation Form
- Also Useful for Analysis of FF Circuits

$$Q(t+1) = D$$

$$Q(t+1) = J\bar{Q}(t) + \bar{K}Q(t)$$

$$Q(t+1) = T \oplus Q(t) = T\bar{Q}(t) + \bar{T}Q(t)$$

D FLIP-FLOPS with ASYNCHRONOUS RESET



(b) Graphic symbol

R	C	D	Q	Q'
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Synchronous Sequential Circuit

- Three Methods of Analysis Considered Here
 1. State Equations (entire circuit)
 2. State Table
 - Concept of Present-State and Next-State
 3. State Diagram
 - Deterministic Finite State Automata

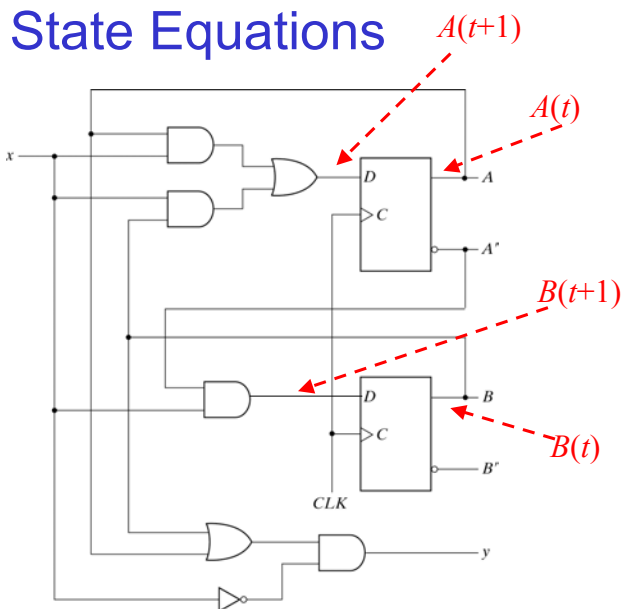


Fig. 5-15 Example of Sequential Circuit

State Equations

$$A(t+1) = A(t)x(t) + B(t)x(t)$$

$$B(t+1) = \bar{A}(t)x(t)$$

$$y(t) = [A(t) + B(t)]\bar{x}(t)$$

Present State (PS) – $A(t)B(t)$

Next State (NS) – $A(t+1)B(t+1)$

State Table

Present State		Input	Next State		Output
<i>A</i>	<i>B</i>		<i>A</i>	<i>B</i>	
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Alternative State Table

Present State	Next State		Output	
	$x=0$	$x=1$	$x=0$	$x=1$
AB	AB	AB	y	y
00	00	01	0	0
01	00	11	1	0
10	00	10	1	0
11	00	10	1	0

State Diagram

