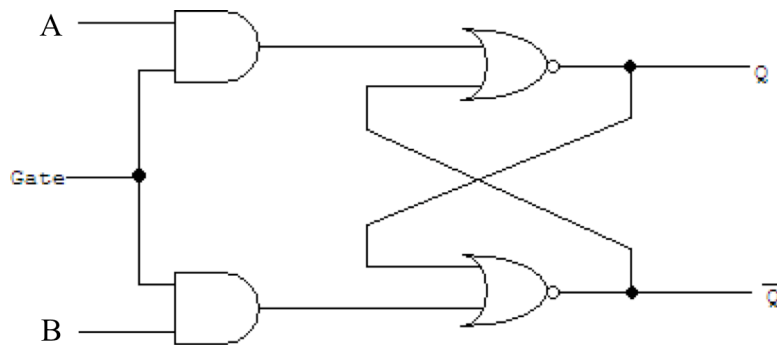


Laboratory 10
CSE 3381
Latches and Flip-Flops

Parts Required: 1 each of 7402, 7404, 7408, 7476

This experiment will allow the student to gain an understanding of how level-sensitive latches and edge-triggered flip-flops function.

PART 1: Construct the AB latch shown in the following diagram using a 7402 and a 7408 and verify the characteristic table by testing all possible inputs and recording the output values. HINT: your table should have 5 rows similar to Figure 5.5 in the textbook.



PART 1 PRELAB: Construct the characteristic table (everything but the outputs) that you will fill in by making measurements in the lab.

LAB INSTRUCTOR'S INITIALS: _____

PART 1 DEMONSTRATION: Show the lab instructor that your circuit operates properly for all inputs.

LAB INSTRUCTOR'S INITIALS: _____

PART 2: Write a Verilog model of the latch given above. Your model should consist of 2 modules; a testbench module that instantiates the latch and provides all possible inputs and a module that implements the latch itself. The latch module can be written as an instantiation of gate primitives. Put delays in for each gate. For the AND gates use a delay of #10, for the top NOR use a delay of #8 and for the bottom NOR use a delay of #5. Your output waveform should verify the results that you recorded in your table in PART 1.

PART 2 PRELAB: Show the lab instructor that you already have your Verilog code written by bringing in a print-out with a listing of the code. You must have separate testbench and latch modules for full-credit. Your Verilog doesn't need to be functional for PRELAB credit (although I highly recommend you get your Verilog working ahead of time so you will know what your measurements should be in PART 1).

LAB INSTRUCTOR'S INITIALS: _____

PART 2 DEMONSTRATION: Show the lab instructor that your Verilog simulation produces a waveform that agrees with your measurements in PART 1.

LAB INSTRUCTOR'S INITIALS: _____

PART 3: Verify the operation of a JK-flip-flop on by using a 7476 (DUAL JK Flip-Flop) chip. You will wire up the JK flip-flop to operate in normal mode, (remember to do "something" with preset and clear inputs) and you will construct a characteristic table similar to the one in Table 5-1 in the text, however; you will have two entries for the top and bottom rows, one each for $Q(t)=0$ and $Q(t)=1$.

PART 3 LAB DEMONSTRATION: Show the lab instructor that your circuit operates properly for all inputs.

LAB INSTRUCTOR'S INITIALS: _____

PART 4: Construct a D flip-flop and a T flip-flop using the 7476 and any of the other parts listed at the top of this page. Verify the functionality of the D and T flip-flop by constructing and measuring their characteristic tables.

PART 4 PRELAB: Neatly draw the circuit diagrams for the T and D flip-flops based on the JK flip-flop and other gates.

LAB INSTRUCTOR'S INITIALS: _____

LAB DEMONSTRATION: Show the lab instructor that your circuits operate properly for all inputs.

POST LAB REPORT: Include your neatly drawn schematics and the PRE-LAB sheet with the lab instructor's initials.