

Laboratory 6  
CSE 3381  
Structural Modeling - Cadence Verilog

This experiment will serve as an introduction to the use of the Cadence Verilog simulation environment and as a design. You should print out this experiment before going to the lab so that you can obtain the lab instructor's initials where needed.

PART 1: Go through the tutorial that walks you through using Cadence Verilog and the waveform viewer using the example circuit we discussed in class. When the final waveform screen is displayed, have the lab instructor come by and initial to verify that you have done this part. You should also capture this window and paste it in a word document for use in your final report (Alt-PrtScr is used to copy a window to the copy buffer).

LAB INSTRUCTOR'S INITIALS: \_\_\_\_\_

PART 2: You will design a student ID number decoder circuit. This circuit will have four inputs A, B, C, and D and it will have four outputs F1, F2, F3, and F4. If your student ID has less than 8 digits, assume there are enough leading zeros to make it an 8-digit number. Everyone's circuit will be different since everyone's student ID is unique.

The four inputs will accept the binary value of a single digit (0-9) with A being the MSb and D being the LSb. The outputs will function as follows:

F1 is to be a logic 1 if the input digit is one of the digits in the first 3 digits (reading from left to right) of your student ID, otherwise it is to be a logic 0.

F2 is to be a logic 1 if the input digit is one of the digits in the fourth or fifth position of your student ID, otherwise it will be a logic 0.

F3 is to be a logic 1 if the input digit is one of the digits in the last three positions of your student ID number, otherwise it is a zero.

F4 is to be a logic 1 if the input is any of the digits in your student ID number, otherwise it is a zero.

If an invalid value is entered (an illegal BCD value), all outputs should be at logic 0.

**PRELAB:**

You are to generate the minimized expressions for F1, F2, F3, and F4 BEFORE the laboratory starts. This should be done by using four Karnaugh maps and writing the corresponding simplified equation under them. You should show these to the Lab Instructor at the beginning of class and she/he will initial below to indicate you have done the Prelab assignment. You may keep the maps and equations to turn in with your final report. Your final report should also include this sheet to show that you received the

initials. If your Prelab maps and/or equations are wrong, you should put the corrected versions in your final report.

LAB INSTRUCTOR'S INITIALS: \_\_\_\_\_

**DEMONSTRATION:** You are to implement a verilog module that contains the ID decoder circuit and a separate module that contains a testbench. You should ensure that your testbench tests all possible four-bit combinations as input. You may implement the Verilog module as either a structural netlist or using Boolean expressions, or some combination of the two.

You should capture the waveform file and save it for inclusion in your final report. When your final waveform screen show it to the lab instructor for sign off below.

LAB INSTRUCTOR'S INITIALS: \_\_\_\_\_

**FINAL REPORT:** Your final report is due the following class period and should include a discussion of any problems you had with the lab and how they were resolved. It should also contain the two waveform screen captures described above, a listing of your Verilog source code, and your design information (i.e. the maps, logic equations, circuits if drawn, etc.).