Synthesis Example with Synopsys Design Compiler

Hierarchical Design (top level)

```
module ripple4 (SUM, A, B);
   input [3:0] A, B;
   output [4:0] SUM;

   full_add u0 (c1, SUM[0], A[0], B[0], 1'b0);
   full_add u1 (c2, SUM[1], A[1], B[1], c1);
   full_add u2 (c3, SUM[2], A[2], B[2], c2);
   full_add u3 (SUM[4], SUM[3], A[3], B[3], c3);
endmodule
```

Hierarchical Design (middle level)

```
module full_add (COUT, S, A, B, CIN);
   input A, B, CIN;
   output COUT, S;
   maj_circ u0 (COUT, A, B, CIN);
   sum u1 (S, A, B, CIN);
endmodule
```

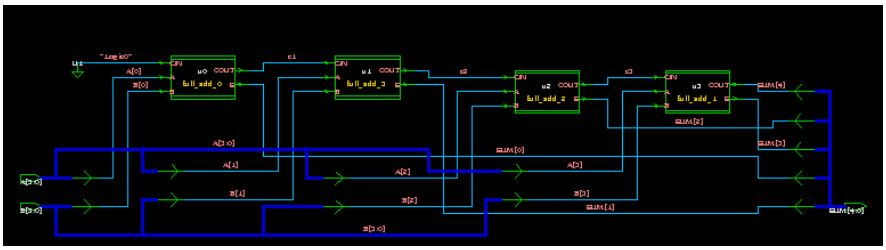
Hierarchical Design (lowest level)

```
module maj_circ (Y, A, B, C);
   input A, B, C;
   output Y;
   and u0 (x1, A, B);
   and u1 (x2, A, C);
   and u2 (x3, B, C);
   or u3 (Y, x1, x2, x3);
endmodule
module sum (S, A, B, CIN);
   input A, B, CIN;
   output S;
   assign S = A ^ B ^ CIN;
endmodule
```

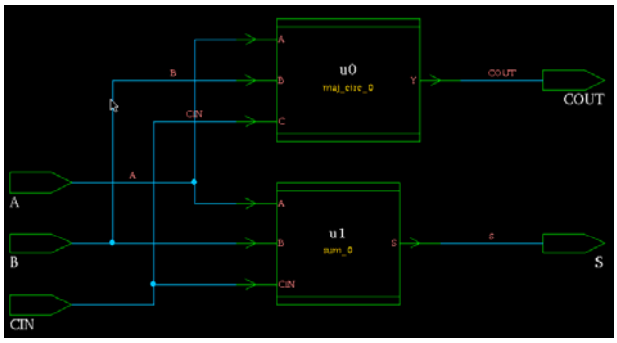
`.synopsys_dc.setup` Script

```
# Example Setup File

# Design Information
set designer "Mitch Thornton"
set company "SMU"

# Setup cell libraries
set search_path
"/usr/local/synopsys/syn.latest/libraries/syn/"
set target_library "lsi_10k.db"
# Designware
set synthetic_library "standard.sldb
dw_foundation.sldb"
set link_library "* $target_library
$synthetic_library"
set symbol_library "lsi_10k.sdb"

define_design_lib MY_WORK -path ./WORK
```

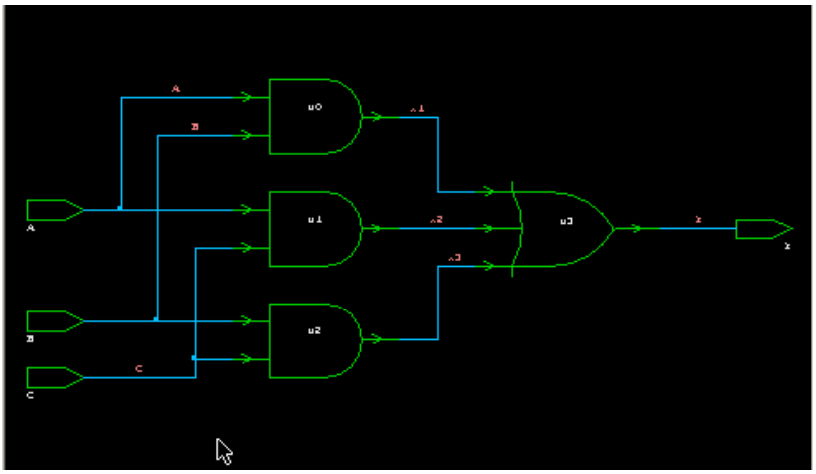
`circuit.v` Schematic (unmapped)



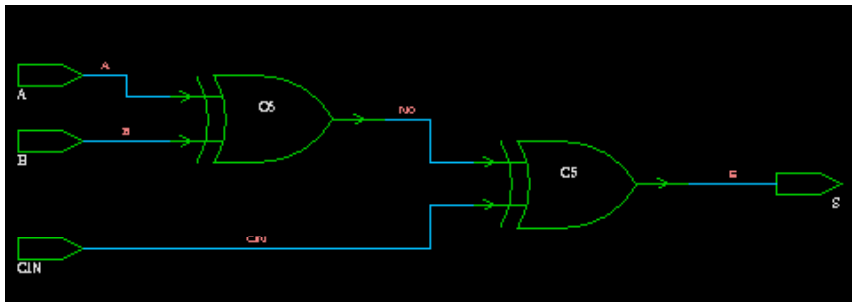
`full_add.v` Schematic (unmapped)



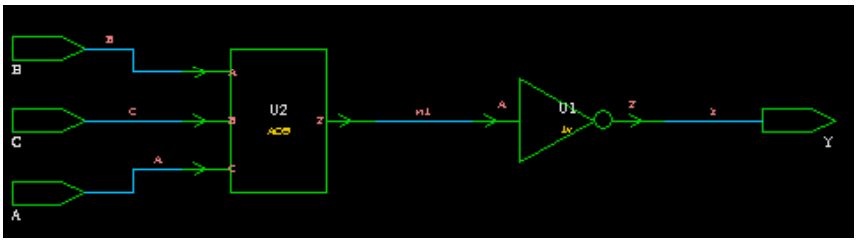
`maj_circ.v` Schematic (unmapped)

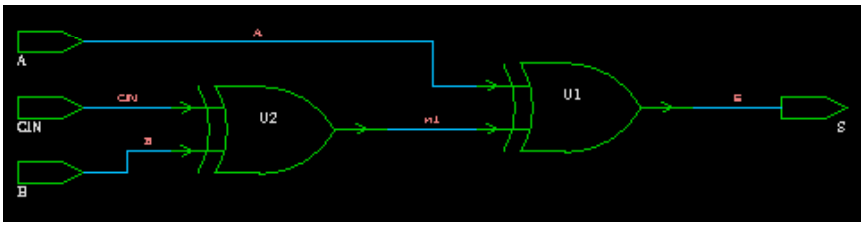


sum.v Schematic (unmapped)



maj_circ.v & **sum.v** Schematic (mapped to **lsi_10k**)





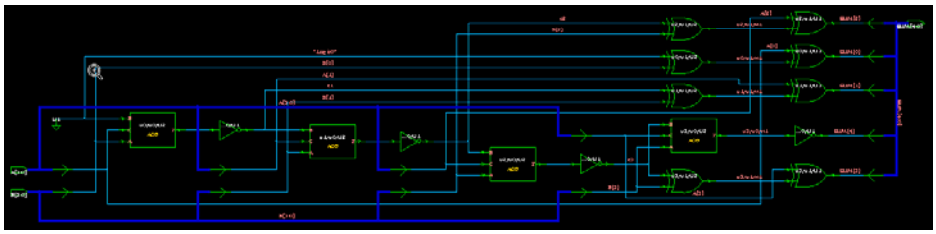
AO5 Cell

```
cell(AO5) {
 area : 3;
 pin(A) {
  direction : input;
  capacitance : 2;
 }
 pin(B) {
  direction : input;
  capacitance : 2;
 }
 pin(C) {
  direction : input;
  capacitance : 1;
 }
 pin(Z) {
  direction : output;
  function : "((A B)+(A C)+(B C))'";
  timing() {
   intrinsic_rise : 1.12;
   intrinsic_fall : 0.45;
   rise_resistance : 0.2612;
   fall_resistance : 0.0788;
   slope_rise : 0.0;
   slope_fall : 0.0;
   related_pin : "A";
  }
  timing() {
   intrinsic_rise : 1.12;
   intrinsic_fall : 0.45;
   rise_resistance : 0.2612;
   fall_resistance : 0.0788;
   slope_rise : 0.0;
   slope_fall : 0.0;
   related_pin : "B";
  }
  timing() {
   intrinsic_rise : 1.12;
   intrinsic_fall : 0.45;
   rise_resistance : 0.2612;
   fall_resistance : 0.0788;
   slope_rise : 0.0;
   slope_fall : 0.0;
   related_pin : "C";
  }
 }
}
```

IV Cell

```
cell(IV) {
 area : 1;
 pin(A) {
  direction : input;
  capacitance : 1;
 }
 pin(Z) {
  direction : output;
  function : "A'";
  timing() {
   intrinsic_rise : 0.38;
   intrinsic_fall : 0.15;
   rise_resistance : 0.1443;
   fall_resistance : 0.0589;
   slope_rise : 0.0;
   slope_fall : 0.0;
   related_pin : "A";
  }
 }
}
```

ripple4.v Flattened (ungrouped) (mapped to **lsi_10k**)



Timing Report

input external delay	0.00	0.00 f
B[0] (in)	0.00	0.00 f
u0/u0/U2/Z (AO5)	1.38	1.38 r
u0/u0/U1/Z (IV)	0.33	1.71 f
u1/u0/U2/Z (AO5)	1.38	3.09 r
u1/u0/U1/Z (IV)	0.33	3.42 f
u2/u0/U2/Z (AO5)	1.38	4.80 r
u2/u0/U1/Z (IV)	0.33	5.12 f
u3/u1/U2/Z (EO)	1.19	6.31 f
u3/u1/U1/Z (EO)	1.06	7.37 f
SUM[3] (out)	0.00	7.37 f
data arrival time	7.37	

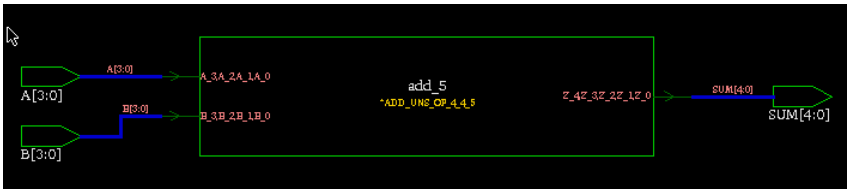
```
****************************************
Report : area
Design : ripple4
Version: A-2007.12-SP5
Date   : Thu Oct  2 10:35:21 2008
****************************************

Library(s) Used:

    lsi_10k (File: /usr/local/synopsys/syn.latest/libraries/syn/lsi_10k.db)

Number of ports:            13
Number of nets:             25
Number of cells:            16
Number of references:        3

Combinational area:       40.000000
Noncombinational area:     0.000000
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:          40.000000
Total area:               undefined
```

```
Information: The cells in your design are not characterized for internal power. (PWR-229)

Operating Conditions:
Wire Load Model Mode: top


Global Operating Voltage = 5
Power-specific unit information :
   Voltage Units = 1V
   Capacitance Units = 0.100000ff
   Time Units = 1ns
   Dynamic Power Units = 100nW    (derived from V,C,T units)
   Leakage Power Units = Unitless


  Cell Internal Power  =   0.0000 nW    (0%)
  Net Switching Power  =   4.1476 uW  (100%)
                  ---------
Total Dynamic Power    =   4.1476 uW  (100%)

Cell Leakage Power     =   0.0000
```

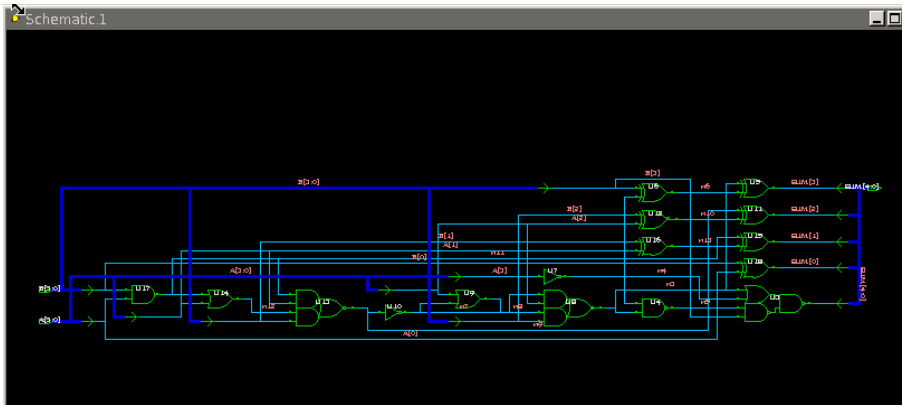
Behavioral Design

```
module ripple4 (SUM, A, B);
   input [3:0] A, B;
   output [4:0] SUM;

   assign SUM = A + B;
endmodule
```

circuit1.v Schematic (unmapped)



Circuit1.v schematic



Timing Report

input external delay	0.00	0.00 f
B[0] (in)	0.00	0.00 f
U17/Z (AN2)	0.93	0.93 f
U14/Z (OR2)	0.91	1.84 f
U13/Z (AO2)	1.34	3.18 r
U10/Z (IV)	0.27	3.45 f
U9/Z (OR2)	0.91	4.35 f
U8/Z (AO2)	1.60	5.96 r
U4/Z (ND2)	0.22	6.17 f
U3/Z (EON1)	0.87	7.04 f
SUM[4] (out)	0.00	7.04 f
data arrival time	7.04	

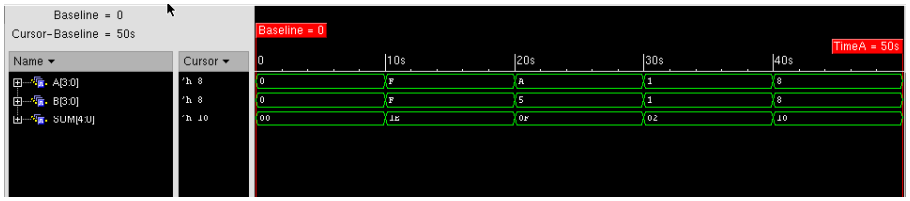
```
****************************************
Report : area
Design : ripple4
Version: A-2007.12-SP5
Date   : Thu Oct  2 10:56:09 2008
****************************************

Library(s) Used:

   lsi_10k (File: /usr/local/synopsys/syn.latest/libraries/syn/lsi_10k.db)

Number of ports:            13
Number of nets:             24
Number of cells:            16
Number of references:        8

Combinational area:       37.000000
Noncombinational area:     0.000000
Net Interconnect area:     undefined  (No wire load specified)

Total cell area:          37.000000
Total area:               undefined
```

```
Information: The cells in your design are not characterized for internal power. (PWR-229)

Operating Conditions:
Wire Load Model Mode: top


Global Operating Voltage = 5
Power-specific unit information :
   Voltage Units = 1V
   Capacitance Units = 0.100000ff
   Time Units = 1ns
   Dynamic Power Units = 100nW    (derived from V,C,T units)
   Leakage Power Units = Unitless


  Cell Internal Power  =   0.0000 nW    (0%)
  Net Switching Power  =   4.0869 uW  (100%)
                   ---------
Total Dynamic Power    =   4.0869 uW  (100%)

Cell Leakage Power     =   0.0000
```

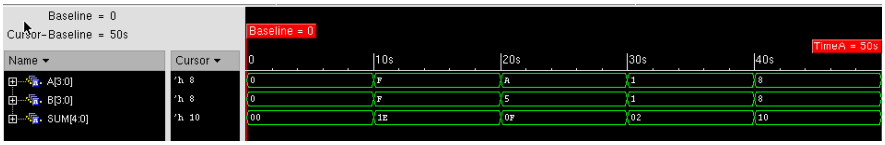
Testbench Module for **`ripple4.v`**

```
// Stimulus for 4-bit ripple carry adder
module top;

  reg [3:0] A, B;
  wire [4:0] SUM;

  // Instantiate adder
  ripple4 u0 (SUM, A, B);

  //Begin simulation
  initial
    begin
      $stop;   // halt in order to open cadence windows
      A=4'h0; B=4'h0;
      #10
      A=4'hf; B=4'hf;
      #10
      A=4'ha; B=4'h5;
      #10
      A=4'h1; B=4'h1;
      #10
      A=4'h8; B=4'h8;
      #10
      $stop;
    end
endmodule
```

Cadence Simulations



`top.v` (structural)



`top1.v` (behavioral)