BOOK ERRATA

(for errors not listed here, please notify Mitch Thornton: mitch@lyle.smu.edu)

1. page 25, figure 1.26 0'b0 should be 1'b0
2. page 28, figure 1-29: {q[6:0],si} move so doesn't overlap top net
3. page 69, figure 2-15: change "**`always @(pstate)`**" to be
   "**`always @(pstate or zero or cnt_eq)`**"
4. page 68, section 2.7.2: change second sentence from "Verilog **`always`** blocks that synthesize into registered logic are those that utilize the Verilog keywords **`posedge`** or **`negedge`** in the signal activation lists…." to "Verilog **`always`** blocks that synthesize into registered logic are those that utilize the Verilog keywords **`posedge`** or **`negedge`** *to modify a clock* input in the signal activation lists…."