Chapter 2

Multiprocessors Interconnection Networks
2.1 Interconnection Networks
Taxonomy

Interconnection Network

Static
- 1-D
- 2-D
- HC

Dynamic
- Bus-based
  - Single
  - Multiple
- Switch-based
  - SS
  - MS
  - Crossbar
2.2 Bus-Based Dynamic Interconnection Networks

• Single Bus Systems
  – Simplest way to connect multiprocessor systems.
  – The use of local caches reduces the processor-memory traffic.
  – Size of such system varies between 2 and 50 processors.
  – Single bus multiprocessors are inherently limited by:
    • Bandwidth of bus.
    • 1 processor can access the bus.
    • 1 memory access can take place at any given time.
2.2 Bus-Based Dynamic Interconnection Networks

- Single Bus Systems

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2.2 Bus-Based Dynamic Interconnection Networks

- **Multiple Bus Systems**
  - Several parallel buses to interconnect multiple processors and multiple memory modules.
  - Many connection schemes are possible.
  - Examples:
    - Multiple Bus with Full Bus – Memory Connection (MBFBMC).
    - Multiple Bus with Single Bus – Memory Connection (MBSBMC).
    - Multiple Bus with Partial Bus – Memory Connection (MBPBMCC).
    - Multiple Bus with Class-based Bus – Memory Connection (MBCBMC).
2.2 Bus-Based Dynamic Interconnection Networks

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2.2 Bus-Based Dynamic Interconnection Networks

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2.2 Bus-Based Dynamic Interconnection Networks

- Multiple Bus Systems:
  - Multiple Bus with Class-based Memory Connection (MBCBMC).
2.2 Bus-Based Dynamic Interconnection Networks

• Bus Synchronization
  – A bus can be synchronous:
    • Time for any transaction is known in advance.
  – A bus can be asynchronous:
    • Depends on the availability of data and readiness of devices to initiate bus transactions.
  – Bus arbitration logic is required to resolve bus contention when more than 1 processor compete to access the bus in single bus multiprocessor.
    • Process of passing mastership from 1 processor to another is called handshaking
      – Requires a bus request and a bus grant.
2.2 Bus-Based Dynamic Interconnection Networks

• Bus Synchronization
  – Bus arbitration logic uses a predefined priority scheme:
    • Random
    • Simple rotating
    • Equal priority
    • Least Recently Used (LRU)
2.3 Switch-Based Interconnection Networks

– Crossbar Networks

• Provide simultaneous connections among all its inputs and all its outputs.

• A Switching Element (SE) is at the intersection of any 2 lines extended horizontally or vertically inside the switch.

• It is a non-blocking network allowing multiple input-output connection pattern to be achieved simultaneously.
2.3 Switch-Based Interconnection Networks

– Crossbar Networks

Straight Switch Setting

Diagonal Switch Setting
2.3 Switch-Based Interconnection Networks

- Single-Stage Networks
  - A single stage of SE exists between the inputs and outputs of the network.
  - Possible settings of a 2x2 SE are:

    Straight  Exchange  Upper-broadcast  Lower-broadcast
2.3 Switch-Based Interconnection Networks

• Multistage Interconnection Networks (MINs)
  – A MIN consists of a number of stages each consisting of a set of 2x2 SEs.
  – Stages are connected to each other using Inter-Stage Connection (ISC) pattern.
  – In MINs the routing of a message from a given source to a given destination is based on the destination address (self-routing).
2.3 Switch-Based Interconnection Networks

- Multistage Networks (MINs)
2.3 Switch-Based Interconnection Networks

• Blockage in Multistage Interconnection Networks
  – Blocking networks:
    • when an interconnection between a pair of input/output is currently established, the arrival of a request for a new interconnection between 2 arbitrary unused input and output may or may not be possible.
2.3 Switch-Based Interconnection Networks

• Blockage in Multistage Interconnection Networks
  – Rearrangeable networks:
    • Always possible to rearrange already established connections in order to make allowance for other connections to be established simultaneously
2.3 Switch-Based Interconnection Networks

- Blockage in Multistage Interconnection Networks
  - Rearrangeable networks
2.3 Switch-Based Interconnection Networks

• Blockage in Multistage Interconnection Networks
  – Non-blocking networks:
    • In presence of a currently established connection between any pair of input/output, it is always possible to establish a connection between any arbitrary unused pair of input/output.
2.3 Switch-Based Interconnection Networks

• Blockage in Multistage Interconnection Networks
  – Non-blocking networks:
2.3 Switch-Based Interconnection Networks

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2.4 Static Interconnection Networks

- Have fixed paths, unidirectional or bi-directional, between processors.
- Types:
  - Completely connected networks: Number of links: $O(N^2)$, delay complexity: $O(1)$. 

![Diagram of a completely connected network](image-url)
2.4 Static Interconnection Networks

– Limited Connection Networks:
  • Linear arrays
  • Ring (Loop) networks
  • Two-dimensional arrays
  • Tree networks
  • Cube network
2.4 Static Interconnection Networks

- Linear arrays
- Ring (Loop) networks
- Two-dimensional arrays
- Tree networks
- Cube network
2.4 Static Interconnection Networks

– Cube Connected Networks:
  • Patterned after the n-cube structure
  • In an n-cube, every processor is connected to n others
  • Ex: a 4-cube:
2.4 Static Interconnection Networks

– Mesh Connected Networks:

Example 3X3X2 mesh network
### 2.5 Analysis and Performance Metrics

#### Dynamic Networks

<table>
<thead>
<tr>
<th>Networks</th>
<th>Delay</th>
<th>Cost</th>
<th>Blocking</th>
<th>Degree of FT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus</td>
<td>$O(N)$</td>
<td>$O(1)$</td>
<td>Yes</td>
<td>0</td>
</tr>
<tr>
<td>Multiple-bus</td>
<td>$O(mN)$</td>
<td>$O(m)$</td>
<td>Yes</td>
<td>$(m-1)$</td>
</tr>
<tr>
<td>MIN</td>
<td>$O(\log N)$</td>
<td>$O(N\log N)$</td>
<td>Yes</td>
<td>0</td>
</tr>
<tr>
<td>Crossbar</td>
<td>$O(1)$</td>
<td>$O(N^2)$</td>
<td>No</td>
<td>0</td>
</tr>
</tbody>
</table>
## 2.5 Analysis and Performance Metrics

- **Static Networks**

<table>
<thead>
<tr>
<th>Networks</th>
<th>Degree (d)</th>
<th>Diameter (D)</th>
<th>Cost (No. of links)</th>
<th>Symmetry</th>
<th>Worst Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCNs</td>
<td>N-1</td>
<td>1</td>
<td>N(N-1)/2</td>
<td>Yes</td>
<td>1</td>
</tr>
<tr>
<td>Linear array</td>
<td>2</td>
<td>N -1</td>
<td>N -1</td>
<td>No</td>
<td>N</td>
</tr>
<tr>
<td>Binary tree</td>
<td>3</td>
<td>2(⌊Log₂N⌋-1)</td>
<td>N -1</td>
<td>No</td>
<td>Log₂ N</td>
</tr>
<tr>
<td>n-cube</td>
<td>Log₂ N</td>
<td>Log₂ N</td>
<td>nN/2</td>
<td>Yes</td>
<td>Log₂ N</td>
</tr>
<tr>
<td>2D-mesh</td>
<td>4</td>
<td>2(n-1)</td>
<td>2(N-n)</td>
<td>No</td>
<td>√N</td>
</tr>
<tr>
<td>K-ary n-cube</td>
<td>2n</td>
<td>N/⌊k/2⌋</td>
<td>n x N</td>
<td>Yes</td>
<td>k x log₂ N</td>
</tr>
</tbody>
</table>
2.6 Summary

- Different topologies used for interconnecting multiprocessors were discussed.
- Taxonomy for interconnection networks based on their topology is introduced.
- Dynamic and static interconnection schemes have been studied.
- A number of basic performance aspects related to both dynamic and static interconnection networks have been introduced.