FAVoR: Formal Arithmetic Circuit Verification Research

INTELLECTUAL MERIT

"*Verification has become the dominant cost in the modern design process*." according to the 2001 ITRS (The International Technology Roadmap for Semiconductors). In particular, arithmetic circuits are well-known for difficulty in functional verification. In the early 1990's public awareness of the importance of design verification was increased due to the Pentium division bug in Intel's microprocessor. Arithmetic circuits tend to present harder cases for emerging verification methods such as equivalence checkers and theorem provers, because the canonic representation forms tend to be very large.

It is clear that one approach for design validation is not emerging as a single solution. Recent scientific publications support the fact that integrated approaches for design verification must be used and discussions with industry personnel support this as well. Instead of focusing on a single approach one very important aspect of this work will be the demonstration of what types of verification approaches should be used for arithmetic circuits and how these approaches interact.

BROADER IMPACT

Arithmetic intensive circuits are being incorporated in many consumer devices. Everything from household appliances to automobiles typically contain at least one microcontroller circuit that contains an arithmetic logic unit (ALU). Because verification is a dominant cost factor and arithmetic circuits are hard cases, any progress in reducing time to market and designs costs will have a tremendous impact on society in terms of providing cheaper and more reliable items.

In terms of local impact, this project will serve as the seed effort to begin establishment of a strong group in computer arithmetic and CAD. The computer science and engineering department at Southern Methodist University has recently added new faculty that complement existing ones and now contains a relatively large number of people with expertise in computer arithmetic and CAD methods. With the funding of this project, many new undergraduate and graduate students would be able to participate in this area in terms of learning and dissemination of expertise. In recent discussions with local industry, heavy encouragement has been received to educate new scientists and engineers with specialized knowledge in verification and arithmetic circuitry. The result of this research would certainly have an impact on these local (but major) companies.

The school of engineering at SMU currently is a national leader in terms of the percentage of female students as compared to the overall population. Currently greater than 30% of undergraduate engineering majors are female and we have an internal goal to reach gender parity within the next five years. Research assistantship funding would allow us to encourage more female undergraduates to pursue graduate degrees and help to achieve the goal of reaching gender parity.

In terms of information dissemination, the proposed PIs each maintain websites that contain a considerable amount of specialized information that is freely available for anyone to access. We plan to make all of our prototype tools available for the public and to publish new results as soon as possible.